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RESEARCH ARTICLE

Design of Low Power Dual Trigger Sequential Circuit

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Abstract— A large portion of the on chip power is consumed by the clock system which is made of the clock distribution network and flip-flops. So the objective is to reduce the power consumption. Most of the on chip power is consumed by the clock system which is made of the clock distribution network and flip-flops. The "Conditional Data Mapping Flip Flop" (CDMFF) and "Clocked Pair Shared Implicit Pulsed Flip Flop" (CPSFF) are triggered using single edge of clock. In CPSFF, reducing capacity of the clock load by minimizing number of clocked transistor was elaborated. The drawbacks of single edge clocking system are high transistor count and floating node problem in critical path. Moreover it cannot be used in noise intensive environment. The CDMFF and CPSFF are triggered using single edge clocking system. Here, the design of a Dual triggered CMOS circuit is proposed. The objective is to reduce the number of clocked transistors and switching activities, thereby reducing the power dissipation. The proposed design is implemented in Microwind 3.1 and simulated using DSCH. The frequency of the Dual triggered CMOS circuit is only half of the clock frequency of the single edge triggered CMOS circuit. Simulation analysis shows that the Dual triggered CMOS circuit reduces switching activities by about 40%, thus reducing dynamic power dissipation. Hence it is suitable for using in high performance and low power environments.

Key Terms: - CDMFF; CPSFF

I. INTRODUCTION

The System-On-Chip (SoC) design is integrating hundreds of millions of transistors on one chip, whereas packaging and cooling only have a limited ability to remove the excess heat. All of these results in power consumption being the bottleneck in achieving high performance and it is listed as one of the top three challenges in ITRS 2008. The clock system, which consists of the clock distribution network and sequential elements (flip-flops and latches), is one of the most power consuming components in a VLSI system. It accounts for 20% to 40% of the total power dissipation in a system.

As a result, reducing the power consumed by flip-flops will have a deep impact on the total power consumed. A large portion of the on chip power is consumed by the clock drivers. Caution must be paid to reduce clock load when designing a clocking system. There is a wide selection of flip-flops in the literature. Many contemporary microprocessors selectively use master-slave and pulsed-triggered flip-flops. Traditional master-slave single-edge flip-flops, for example, transmission gated flip-flop, are made up of two stages, one master and one slave. Another edge-triggered flip-flop is the sense amplifier-based flip-flop (SAFF).

All of these hard edged-flip-flops are characterized by a positive setup time, causing large D-to-Q delays. Alternatively, pulse-triggered flip-flops reduce the two stages into one stage and are characterized by the soft edge property. 95% of all static timing latching on the Itanium 2 processor use pulsed clocking.

Pulse triggered flip-flops could be classified into two types, implicit-pulsed and explicit-pulsed, for example, the implicit pulse-triggered data-close-to-output flip-flops (ip-DCO) and the explicit pulse-triggered data-close-to-output flip-flops (ep-DCO).

A transmission-gate master-slave latch pair has the largest internal race margin, lowest energy consumption, and has energy-delay product comparable to much faster pulse-triggered latches. A common design approach for minimizing energy consumption in flip-flops is to reduce the switching component of energy,

$$E = a.C_{sw}.V_{swing}.V_{DD..}$$

Based on this formula, energy consumption can be reduced by simply minimizing each of the terms in the product expression. However, lowering the supply voltage results in increased flip-flop delay, so the delay has to be included in the optimization metric. Clocked capacitances should be minimized in order to reduce the clock load. The total circuit area depends on the size of the output load and required driving strength. With energy reduction in clocked nodes and the output load, sizing for optimal performance under these energy constraints reduces to optimizing the speed of the flip-flop's critical path. This closely approximates the sizing for optimal energy-delay product (EDP).The circuit is optimized to drive an output load of 4 standard loads (SL), where SL is the input capacitance of a unity buffer from standard cell library. While 4SL load is most common effective fan-out in synthesized low energy systems, sizing procedure can be extended to any load. The method of logical effort is used in transistor size optimization.

The rest of the paper is organized as follows. Section II describes the implementation of our identification method. Section III presents experimental results that illustrate the effectiveness of this approach. Section IV compares the results with existing method and the Section V includes the concluding remarks.

II. CONDITIONAL DATA MAPPING FLIP-FLOP

A. Methods of Low Power Design of a Clocking System

In Power consumption is determined by several factors including frequency f, supply voltage V, data activity α, capacitance C, leakage and short circuit current

$$P=P_{dynamic} + P_{short\ circuit} + P_{leakage}$$

In the above equation, dynamic power $P_{dynamic}$ is also called the switching power,

$$P_{dynamic}=\alpha CV^2f.$$

$P_{leakage}$ is the short circuit power which is caused by the finite rise and fall time of input signals, resulting in both the pull up network and pull down network to be ON for a short while .$P_{short\ circuit} = I_{short\ circuit} V_{dd}$

$P_{leakage}$ is the leakage power. With supply voltage scaling down, the threshold voltage also decreases to maintain performance. However, this leads to the exponential growth of the subthreshold leakage current. Subthreshold leakage is the dominant leakage now.

$$P_{leakage}= I_{leakage}V_{dd}.$$

B. Factors that lowering the power Consumption

Based on these factors, there are various ways to lower the power consumption shown as follows.

1) Double Edge Triggering:

Using half frequency on the clock distribution network will save approximately half of the power consumption on the clock distribution network. However the flip-flop must be able to be double clock edge triggered.

For example, the clock branch shared implicit pulsed flip-flop (CBS-ip DEFF), is a double edge triggered flip-flop. Double clock edge triggering method reduces the power by decreasing frequency f in equation.

2) Using a low swing voltage on the clock distribution network can reduce the clocking power consumption since power is a quadratic function of voltage. To use low swing clock distribution, the flip-flop should be a low swing flip- flop.

For example, low swing double-edge flip-flop (LSDFF) is a low swing flip-flop. In addition, the level converter flip-flop is a natural candidate to be used in low swing environment too. For example, CD-LCFF-ip could be used as a low swing flip-flop since incoming signals only drive nMOS transistors. The low swing method reduces the power consumption by decreasing voltage in equation.

3) There are two ways to reduce the switching activity: conditional operation (eliminate redundant data switching: conditional discharge flip-flop (CDFF)), conditional capture flip-flop (CCFF) or clock gating.

a) Conditional Operation:

For dynamic flip-flops, like hybrid latch flip-flop (HLFF), semidynamic flip-flop (SDFF) , there are redundant switching activities in the internal node. When input stays at logic one, the internal node is kept charging and discharging without performing any useful computation. The conditional operation technique is needed to control the redundant switching.

For example, in CDFF, a feedback transistor is inserted on the discharging path of 1st stage which will turn off the discharging path when D keeps 1. Internal node will not be kept discharging at every clock cycle.

In CCFF, it uses a clocked NOR gate to control an nMOS transistor in discharging path when Q keeps 1. The redundant switching activity is removed in both cases. This reduces the power consumption by decreasing data activity.

b) Clock Gating:

When a certain block is idle, we can disable the clock signal to that block to save power. Gated master slave flip-flop is used. Both conditional operation and clock gating methods reduce power by decreasing switching activity.

4) Using Dual Vt/MTCMOS to reduce the leakage power in standby mode. With shrinking feature size, the leakage current increases rapidly, the MTMOS technique as well as transistor stacking, dynamic body biasing, and supply voltage ramping could be used to reduce leakage standby power consumption .5) Reducing Short Current Power:

Split path can reduce the short current power, since pMOS and nMOS are driven by separate signals.

6) Reducing Capacity of Clock Load:

80% of non-clocked nodes have switching activity less than 0.1. This means reducing power of clocked nodes is important since clocked node has 100% activity. One effective way of low power design for clocking system is to reduce clock capacity load by minimizing number of clocked transistor. Any local clock load reduction will also decrease the global power consumption. This method reduces power by decreasing clock capacity.

2.1 SINGLE EDGE CMOS CIRCUIT - CLOCKED-PAIR SHARED IMPLICIT PULSED FLIP-FLOP

CDFF and CCFF use many clocked transistors. CDMFF reduces the number of clocked transistors but it has redundant clocking as well as a floating node. To ensure efficient and robust implementation of low power sequential element, we propose Clocked Pair Shared flip-flop to use less clocked transistor than CDMFF and to overcome the floating problem in CDMFF. In the clocked-pair-shared flip-flop, clocked pair (N3, N4) is shared by first and second stage.

An always on pMOS, P1, is used to charge the internal node X rather than using the two clocked precharging transistors (P1, P2) in CDMFF.

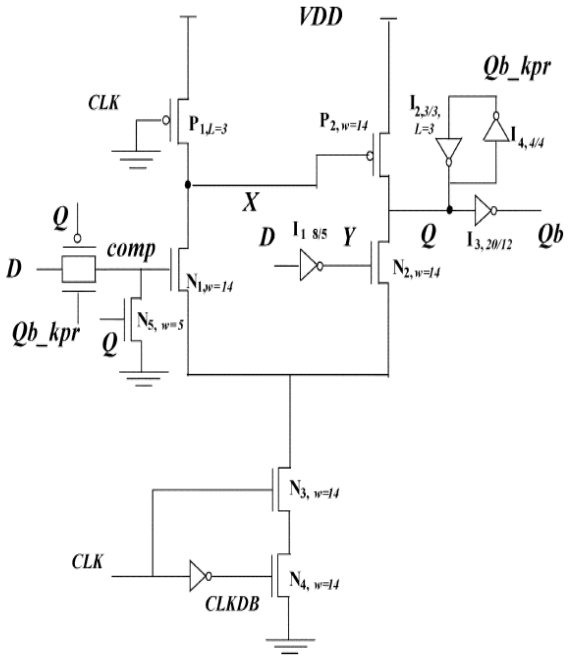

Fig. 2. Single Edge CMOS Circuit -Clocked Pair Shared Flip-Flop

Comparing with CDMFF, a total of three clocked transistors are reduced, such that the clock load seen by the clock driver is decreased, resulting in an efficient design. Further the transistor N7 in the clocked inverter in CDMFF is removed. CPSFF uses four clocked transistors rather than seven clocked transistors in CDMFF, resulting in approximately 40% reduction in number of clocked transistors.

Furthermore the internal node X is connected to Vdd by an always on P1, so X is not floating, resulting in enhancement of noise robustness of node X. This solves the floating point problem in CDMFF. The always ON P1 is a weak pMOS transistor (length=3l). This scheme combines pseudo nMOS with a conditional mapping technique where a feedback signals, comp, controls nMOS N1.

When input D stays 1, Q = 1 , N 5 is on, N1 will shut off to avoid the redundant switching activity at node X as well as any short circuit current. pMOS P2 should pull Q up when D transits to 1. The second nMOS branch (N2) is responsible for pulling down the output of Q if D = 0 and Y = 1. When the clock pulse arrives, pMOS in I1 should turn on nMOS N2 when D = 0.

Although P1 is always ON, short circuit only occurs one time when D makes a transition of 0 to 1 , and the discharge path is disconnected after two gates delay by comp (turning off N1). After that, if D remains at 1, the discharge path is already disconnected by N1; there would be no short circuit.

The clocked-pseudo-nMOS scheme is different from the general idea of conventional pseudo-nMOS logic in that we use clocked transistors in the pull down branch. P1, N1, N3, and N4 should be properly sized to ensure a correct noise margin.

Several low power techniques can be easily incorporated into the new flip-flop. Unlike CDMFF, low swing is possible for CPSFF since incoming low voltage clock does not drive pMOS transistors. Low swing voltage clock signals could be connected to the nMOS transistors N3 and N4, respectively. In addition, it is easy to build double edge triggering flip-flop based on the simple clocking structure in CPSFF. Further CPSFF could be used as a level converter flip-flop automatically, because incoming clock and data signals only drive nMOS transistors.

III. DUAL EDGE TRIGGERED CMOS CIRCUIT

Conventional DEFFs duplicate the area and the load on the inputs. Explicit pulsed DEFFs use external clock pulse generators, which increase the power. In addition, explicit pulsed DEFFs cannot work with dynamic logic. SPGFF uses implicit pulsing; however, it has four internal redundant switching nodes. Unlike SPGFF, DECPFF eliminates the redundant switching activity, however, the number of clocked transistors reaches 21, and the clock branch duplicating structure is complex. To ensure efficient implementation of double-edge clock triggering in an implicit pulsed environment and to overcome the problem with previous implicit pulsed flip-

flops which is the large clock load, a novel clock branch sharing topology is proposed. The sharing concept is similar to the single transistor clocked FF and another clock branch sharing flip-flop. In this new clock branch sharing scheme, Fig. 4.1 (N1, N3), (N2, N4) are shared by the first stage and second stage (in the doted circle). Note that a split path (node X does not drive nMOS N6 of the second stage, which is in the output discharging path) is used to ensure correct functioning after merging. The advantage of this sharing concept is reflected in reducing the number of transistors required to implement the clocking branch of the double-edge triggered implicit-pulsed flip-flops. Without this sharing, the number of clocked transistors would be much larger than the number of transistors used with the sharing concept. Recall that clocked transistors have a 100% activity factor and consume a large amount of power. Reducing the number of clocked transistors is an efficient way to decrease the power. Using Pseudo nMOS (always on pMOS P1) in CBS_ip takes advantage of the fact that D and Qb have inversed polarity resulting from the conditional discharge technique. The discharging path only stays ON for a short while, yielding only a little short circuit current. An inverter is placed after Q, providing protection from direct noise coupling

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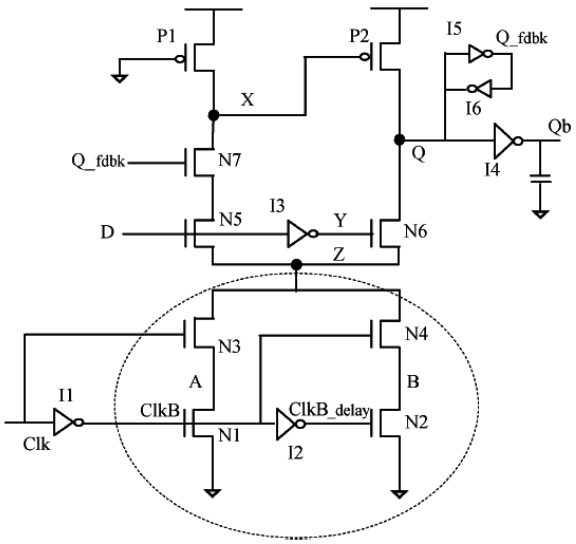

Fig 3. Dual edge CMOS circuit

The double edge triggering operation of the flip-flop is as follows. Q_fdbk is used to control N7. When CLK rises, CLKB will stay high for a short interval of time equal to one inverter delay. During this period, the clocked branch (N1 and N3) turns on and the flip-flop will be in the evaluation period. Note that the other clocked branch (N2 and N4) is disconnected. When CLK falls, CLKB will rise, and CLKB_delay will stay HIGH for one inverter delay period during which the transistors N2 and N4 are both on, and the flip-flop is in the evaluation mode. The first stage in the design is responsible for capturing input transitions of D. The internal node X will discharge causing the outputs Q and Qb to be HIGH and LOW, respectively;N7 turns off by ;

If the input D stays "1"the first stage is disconnected from ground in the later evaluations preventing node X from experiencing redundant switching activity. The second stage, on the other hand, is responsible for capturing the input transitions. In this case, the falling transition of the input will cause the pull down network of the second stage to be ON and, thus, forcing the output nodes Q and Qb to be 0 and 1, respectively. Using a split path in CBS_ip (P2 is driven by X, N2 by Y,respectively), the capacitance on node X is much smaller than that on node Q, which causes a significant difference in propagation delay through the FF. The reason for this is that node X only drives one device, P2. To further reduce latency, clocked inverters I1 and I2 are placed to drive bottom clocked transistors N1 and N2, respectively. Before the clock rising/falling edge, the output of I1/I2 turns on N1, N2, respectively, thus, the internalnodes A and B are discharged to ground before evaluation correspondingly, and this can reduce the discharge time. Though it has four stacked transistors in the first stage, the above methods (split path, and moving the early signals near GND) help to reduce the high stack's negative effect on delay. Using the conditional discharge technique, Q_fdbk turns off N7 in two gate delays, so we need not use a 3-inverter delay in the clock pulse window.

The one inverter window width is sufficient for node X to discharge to ground. The reasons are as follows. First, node X has a much smaller capacitive load than that at Q. Further, we can adjust the one-inverter-delay by

weakening the nMOS in I1 and I2. Note that the nMOS in I2 and I1 control the gate of N1 and N2. Weakening of the Nmos can be achieved by using the width, and increasing the length (L) of the nMOS (since the resistance is proportional to L/W). So, when L increases, the resistance increases. This allows N1 and N2 to stayONlonger after the clock rising/falling edge, respectively, before being turned off by the nMOS in I1and I2, thus, enlarging the pulse width. For the four stacked transistors, N5, N1, N3, and N7, charge sharing may occur when three of them become ON at the same time.

A properly sized always-ON pMOS P1 enables a constant charging path, which reduces the effect of charge sharing. P1,N1, N2, and N3 should be properly sized to ensure a correct noise margin; the value of VOL should be small .In summary, the clock-sharing scheme reduces the number of clocked transistors. The reduction of the number of clocked transistors reduces the switching activity, decreasing the power usage. Also, the pseudo-nMOS replaces the pMOS clocking scheme. In addition, the conditional discharge technique and split path technique are used to reduce redundant switching activity at node X and reduce the short circuit power consumption, respectively.

IV. RESULTS AND DISCUSSION

The simulation results of Single Edge CMOS Circuit and Dual Edge CMOS Circuit.The circuit is drawn and simulated using MICROWIND 3.1 tool and the technology used here is 90nm. The schematic diagram and the output waveforms are shown.

Table 4.1 Performance comparison of Single Edge CMOS Circuit and Double Edge CMOS Circuit

PARAMETER	SINGLE EDGE-CIRCUIT	DOUBLE EDGE-CIRCUIT
Power(μW)	27.718	14.488
Delay(pS)	21.7	20.1
Power Delay Product (PDP) (E-15)	0.601	0.291

POWER ANALYSIS

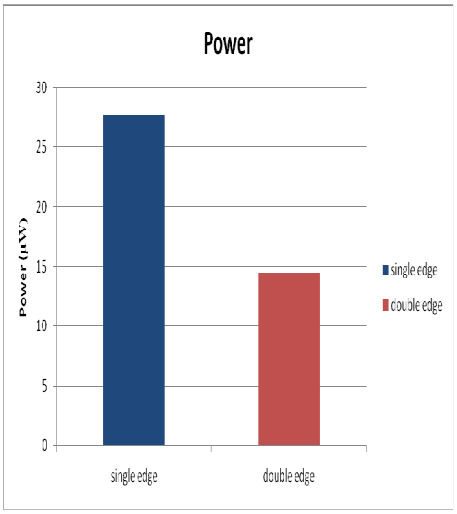

Fig 4. Power Analysis of Single Edge CMOS Circuit and Dual Edge CMOS Circuit

Figure shows the power dissipation of Single Edge CMOS Circuit and Dual Edge CMOS Circuit. The power consumption of Dual Edge CMOS Circuit decreases by 45%

DELAY ANALYSIS

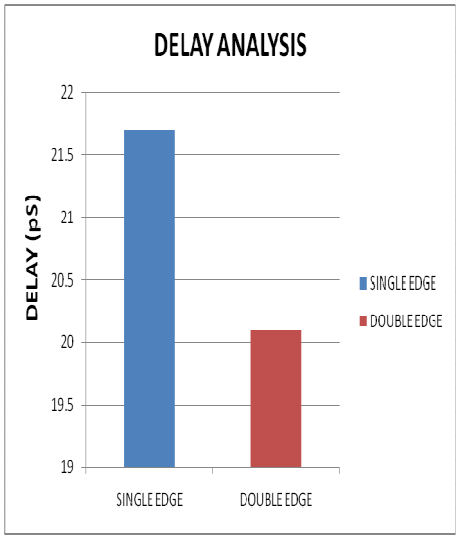

Fig .5 Delay Analyses of Single Edge CMOS Circuit and Dual Edge CMOS Circuit

Figure shows the delay dissipation of Single Edge CMOS Circuit and Dual Edge CMOS Circuit. The power consumption of Dual Edge CMOS Circuit decreases by 7%

POWER DELAY PRODUCT ANALYSIS

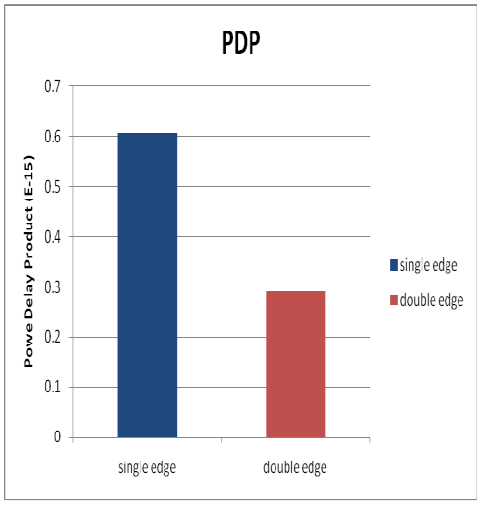

Fig.6 shows the power delay product of Single Edge CMOS Circuit and Dual Edge CMOS Circuit. The power consumption of Dual Edge CMOS Circuit decreases by 45%

V. CONCLUSION

The design of Single Edge CMOS Circuit and Dual Edge CMOS Circuit is designed here. Using Single Edge CMOS Circuit, reducing capacity of the clock load by minimizing number of clocked transistor, is elaborated. Following the approach, the proposed Dual Edge CMOS Circuit reduces local clock transistor number by about 40%. Single Edge CMOS Circuit and Dual Edge CMOS Circuit are designed in MICROWIND 3.1. Comparison

is made for Single Edge CMOS Circuit and Dual Edge CMOS Circuit. Outputs are verified for the input set and performance metrics for these methods are measured and tabulated. Analysis of result shows Dual Edge CMOS Circuit outperforms Single Edge CMOS Circuit in terms of power dissipation and number of clocked transistors.

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