Available Online at www.ijcsmc.com

International Journal of Computer Science and Mobile Computing

A Monthly Journal of Computer Science and Information Technology

ISSN 2320–088X

IJCSMC, Vol. 2, Issue. 4, April 2013, pg.52 – 57

RESEARCH ARTICLE

FPGA Design of Parallel Linear-Phase FIR Digital Filter Using Distributed Arithmetic Algorithm

P. Karthikeyan[1], Dr. Saravanan.R[2]
[1]Assistant Professor, Department of ECE, PSNA College of Engineering & Technology, Dindigul, India
[2]Professor, Department of CSE, PSNA College of Engg and Tech, Dindigul, India

[1]karthickcnp@gmail.com; [2]hodcse@psnacet.edu.in

Abstract— Based on fast FIR algorithms (FFAs), we propose distributed arithmetic algorithm based new parallel FIR filter architectures, which are beneficial to symmetric convolutions in terms of the hardware cost. Multipliers are the major portions in hardware consumption for the parallel FIR filter implementation. The proposed new structures exploit the nature of symmetric coefficients of odd length and further reduce the amount of multipliers required at the expense of additional adders. Exchanging multipliers with adders is advantageous because adders weigh less than multipliers in terms of silicon area, and in addition, the overhead from the increase in adders in preprocessing and post processing blocks stay fixed, not increasing along with the length of the FIR filter, whereas the number of reduced multipliers increases along with the length of the FIR filter.

Key Terms: - FFA Algorithm; Distributed arithmetic algorithm; FIR Filter; Convolution; Digital Signal Processing

Full Text: http://www.ijcsmc.com/docs/papers/April2013/V2I4201309.pdf