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RESEARCH ARTICLE

DESIGN AND ANALYSIS OF POWER EFFICIENT CLOCKED PAIR SHARED FLIP FLOP

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Abstract— In this paper, we examine the problems in the CDN of the flip flop & design an improved CDN oriented Flip-flop which is Clocked Pair Shared Flip Flop (CPSFF). Clock Division Network (CDN)'S plays an important role in the flip flop design and it's the major element in the flip –flop for producing the logical outputs it's much important to design the CDN with low power and area. Power consumption is the main traffic jam of system performance. Low power flip-flops which plays a vital role for the design of low-power digital systems. Flip flops and latches consume a large amount of power due to redundant transitions and clocking system. In addition, the energy consumed by low skew clock distribution network is steadily increasing and becoming a larger fraction of the chip power. Almost, 30% - 60% of total power dissipation in a system is due to flip flops and clock distribution network. In order to achieve a design that is both high performances while also being power efficient, careful attention must be paid to the design of flip flops and latches. We survey a set of flip flops designed for low power and High performance.

Key Terms: - Flip Flop; Clock Division Network; Clocked Pair Shared Flip Flop; Power

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