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RESEARCH ARTICLE

Design of Moderate Speed and Moderate Resolution Successive Approximation Analog to Digital Converter

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***Abstract:** This Paper presents the Design of analog to digital converter (ADC) for low power applications, so here is the selection of right architecture is very crucial. We have chosen successive approximation Analog to Digital Converter because of their compact circuitry as compared with the Flash ADC which makes this SAR ADC inexpensive. Day By Day more and more applications are built on the basis of power consumption so this SAR ADC will be useful for high speed with medium resolution and low power consumption. The Successive Approximation (SAR) architecture is very suitable for data acquisition, it has resolutions ranging from 8 bits to 12 bits and sampling rates ranging from 50 KHz to 50 MHz*

***Keywords:** Successive Approximation Register (SAR), Low power, Resolution, Sampling Rate*

I. Introduction

In many mixed-signal systems, Analog-to-Digital Converters (ADC) are required for interfacing analog signals to digital circuits [8]. Sigma Delta ADC architectures are very useful for lower sampling rate and higher resolution (approximately 12-24 bits). The common applications for Sigma-delta ADC architecture are found in voice band, audio and industrial measurements. The Successive Approximation (SAR) architecture is very suitable for data acquisition, it has resolutions ranging from 8 bits to 12 bits and sampling rates ranging from 50 KHz to 50 MHz. The most effective way to create a Giga rate application with 8 to 16 bit resolution is the pipeline ADC architecture. Here in this we are presenting SAR ADC because in the past few years, more and more applications are built with very stringent

requirements on power consumption. For electronic systems, such as wireless systems or irnplantable devices, the power consumption is becoming one of the most critical factors. SAR ADC is known for its simple structure, thus consuming less power and saving more die size [1].This SAR ADC also use in Ultra Wide Band (UWB) radio technology. UWB receivers require high-speed but low-resolution analog-to-digital converters (ADCs), in the range of 4–5 bits. Pipelined ADCs are used for high-speed, medium-resolution applications. They can provide one conversion per clock period throughput and only a linear scaling in complexity with resolution; however, they rely on operational amplifiers at the heart of the multiplying digital-to-analog converter (MDAC) in each pipelined stage. Because it must be closed loop stable, this amplifier typically uses one or two high gain stages. Unfortunately, in deep-submicron CMOS, the achievable gain per stage is limited because short-channel effects lower $g_m r_0$ for a single transistor, and reduced voltage supplies restrict circuit techniques such as cascading. Thus, there are significant challenges for continued scaling of pipelined ADCs [2]. Thus, this SAR ADCs are commonly used in biomedical acquisition systems due to their low power consumption and simplicity, particularly for simple analog sub-circuits. This SAR ADC consists of sample and hold circuit, a comparator, Successive approximation register and control logic and DAC.

II. Related Work

The paper [1] presents Low power Successive Approximation ADC for MAV'S. Here MAV's is a Micro Air Vehicle system. In communication subsystems such as Micro air vehicles MAV's, it becomes mandatory to design the circuits with low power and low voltage to enhance the system by means of long sustainability and less power consumption with maintenance free operation, especially in the circuits like Analog to Digital Converters (ADCs). In chemical cloud different types of gases are present in that mainly carbon monoxide which are very harmful. MAV is consisting of a sensor it can detect the toxic gases which are released from vehicle. Here sensor signals are analog signals need to convert into digital signals for visualization with the help of Successive Approximation ADC. The analog input frequency is 75MHz and oversampling conversion frequency is 750MHz with 27.4mW low power design is achieved with this technique. This is implemented in 180nm technology [1].

The paper [2] presents ADC for ULTRA WIDEBAND (UWB) radio technology. The Ultra Wide Band radio technology is an emerging technology For very high data rate and Short Distance Wireless communication. UWB receivers require high speed but low resolution analog to digital converter in the range of 4-5 bits. The time-interleaved successive approximation register (SAR) architecture has been chosen due to its simplicity versus flash and its amenability to scaled technologies versus pipelined, which relies on operational amplifiers. In this ADC, there is use of split capacitor array DAC which is used For Increasing the speed and For Reduces the switching energy. This ADC consumes 6mw from 1.2 V supply. This is implemented in 65 nm technology [2].

The paper [3] presents ADC designed for low-power, medium-quality applications such as data acquisition. The requirement is usually to integrate these ADC's with digital signal processors (DSP's) in a low-cost CMOS technology. ADC's that are integrated with a DSP are required to operate in the same range of supply voltage. However, designing an ADC to operate at such a low supply voltage presents a great challenge, which comes from the fact that the threshold voltages of MOSFET devices are relatively high for the given supply voltage ranges even for future CMOS processes. To address this challenge, different techniques have been used to realize ADC's including the use of specialized process that provides low-threshold devices, bootstrap techniques, and switched-op-amp techniques. This ADC consumes 0.34 mW from 1V supply. This technique is implemented in 120 nm process [3].

The paper [4] presents ADC for high speed wire line and wireless communication system. In these applications, low-power and small-area ADCs requiring conversion rates higher than 60 MS/s and a resolution in the range of 7–9 bits are considered an important building block. Among many ADC architectures, successive approximation register (SAR) ADCs have proven to be very efficient for meeting the above requirement of high speed, medium resolution, and low power consumption. In this ADC, which includes a comparator with offset cancellation and uses digital calibration for error correction? This ADC consumes 3.4 mW with the reference 1.0V supply. This ADC is implemented in 65-nm CMOS technology with area of 0.068mm^2[4].

The paper [5] presents ADC for upcoming low energy radios in the ISM (industrial, scientific and medical) radio bands such as low-energy Bluetooth or IEEE 802.15.6 for body-area networks. The successive approximation architecture (SAR) is selected in this work because of the excellent power efficiency The use of simple modulation schemes like OOK, moderate resolutions (e.g. 4 bit up to 8 bit) are sufficient. Data rates are strongly application dependent, but are typically expected in the range of several KS/s (e.g. medical sensor applications like ECG monitoring) up to several MS/s (e.g. audio streaming). This work proposes an architecture that achieves excellent power-efficiency for an 8 bit ADC using sample rates from 1 KS/s up to 10 MS/s. Here By using dedicated 0.5 fF capacitors, asynchronous dynamic logic and a low-complexity design, an energy efficiency of 12 fJ/conversion-step

could be achieved at 10MS/s. Because of the fully dynamic design and a low leakage level of only 6 nW, the excellent efficiency is maintained down to the kS/s range[5].

The paper [6] presents an energy efficient successive-approximation register (SAR) analog-to-digital converter (ADC) for biomedical applications. **I**n the last few years, there has been a growing interest in the design of wireless sensing device for portable, wearable or implantable biomedical applications. These sensing devices are generally used for detecting and monitoring biomedical signals such as electrocardiographic (ECG), electroencephalography (EEG), and electromyography (EMG). Most biomedical signals are often very slow and exhibit limited dynamic range. A typical biomedical sensor interface consists of a band-pass filter, a low-noise amplifier and an analog-to-digital converter (ADC). The digitalization of the sensed biomedical signals is usually performed by ADCs with moderate resolution (8–12 bits) and sampling rate (1–1000 kS/s). This ADC fabricated in 0.18-µm 1P6M CMOS technology also at a 0.6-V supply voltage and a 200-kS/s sampling rate, the ADC achieves a signal-to-noise and distortion ratio of 57.97 dB and consumes 1.04 µW, resulting in a figure of merit of 8.03 fJ/conversion-step. The ADC core occupies an active area of only 0.082 mm[6].

The paper [7] presents a design of ultra-low-power successive approximation register (SAR) analog-to-digital converters (ADC) specially optimized for very low frequency biosensor applications. In this ADC there is a use of two new techniques namely a novel digital-to-analog converter (DAC) switching method suitable for single-ended SAR ADCs; and a counter-based digital control circuitry. The proposed DAC switching method uses only one reference voltage of $V_R/2$ to digitize the signals with the amplitude range of $[0,V_R]$ which can help ADC to digitize input signals larger than V_{DD}. The
prototype 0.35-u m SAR ADC achieves an ENOB of 7.8 bits at 2 kS/s with a total power of 101 nW and a FOM of 227 fJ/conversion-step. The proposed 0.18- m SAR ADC achieves an ENOB of 7.4 bits at 2 kS/s with the overall power consumption of 27 nW and a FOM of 79.9 fJ/conversion-step, while it only consumes 16.5 nW with a FOM of 97.7 conversion-step at 1 kS/s. The proposed ultra-low-power SAR ADC is, therefore, very attractive to be part of the analog front-end circuitry for biosensor applications [7].

III. Proposed Work

Up till now the design of the Successive Approximation Analog to Digital Converter has been implemented with good resolution in particular higher nanometer technology having good sampling rate. So if we implement this SAR ADC with higher sampling rate then the technology will be increased. So we will implement this SAR ADC having Resolution of 8 bit with sampling rate in Mega Samples Per Second in reduction in its nanometer technology. So for designing such Compact Low Power SAR ADC, it provides less chip size also minimization of power takes place. This Proposed SAR ADC will be designed in Tanner Tool V15.0 /ADS Tool. Performance evaluation will be based on the implementation results obtained through this tool.

Generalised Block Diagram of SAR ADC:

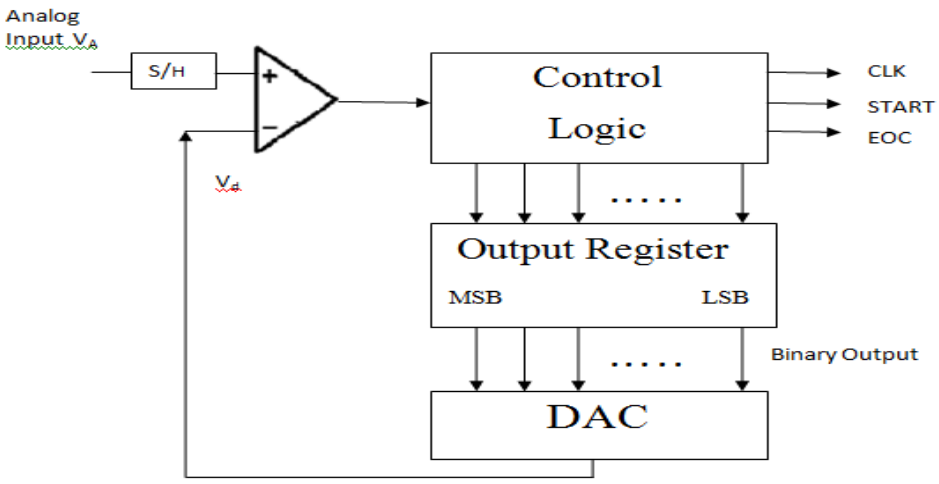

Fig : General Block Diagram of SAR ADC

Advantages:

The main advantage of SAR ADC is good ratio of speed to power. The SAR ADC has compact design compare to flash ADC, which makes SAR ADC inexpensive. This SAR ADC will be useful for high speed with medium resolution and low power consumption.

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