Available Online at www.ijcsmc.com

International Journal of Computer Science and Mobile Computing

A Monthly Journal of Computer Science and Information Technology

ISSN 2320–088X

IJCSMC, Vol. 2, Issue. 8, August 2013, pg.120 – 129

RESEARCH ARTICLE

Low Power Flip-Flop Design for Low Swing LC Resonant Clock Distribution Networks

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Abstract— Low-power design is becoming a crucial design objective due to the growing demand on portable applications and the increasing difficulties in cooling and heat removal. The clock distribution network (CDN) delivers the clock signal which acts as a reference to all sequential elements in the synchronous system. The clock distribution network consumes a considerable amount of power in synchronous digital systems. Resonant clocking is an emerging promising technique to reduce the power of the clock network. The inductor used in resonant clocking enables the conversion of the electric energy stored on the clock capacitance to magnetic energy in the inductor and vice versa. This thesis describes a family of novel low-power flip-flops, which are suitable to work in low power low swing clock distribution networks. They achieve statistical power reduction by eliminating redundant transitions of internal nodes. The Conditional Capturing flip-flop is modified to operate with a low-swing sinusoidal clock. Low-swing resonant clocking achieved around 5.8% reduction in total power with 5.7% area overhead. Modeling the clock network with the existing Low Swing Differential Conditional Capturing Flip-Flop illustrates that low-swing clocking can achieve up to 58% reduction in the power consumption of the resonant clock. In order to achieve further power reduction, low swing sinusoidal clock with Clock Gating is introduced with modification in existing Flip Flops. Simulation results illustrate that by utilizing the proposed approach, more than 80% reduction in power consumption and approximately 85% reduction in noise level can be achieved.

Key Terms: - Clock; Flip-Flop; Low-Swing; Resonant Clock; Low Power; Clock Gated; Clock Distribution Network; Sinusoidal Clocking

Full Text: http://www.ijcsmc.com/docs/papers/August2013/V2I8201333.pdf