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Adaptive Feedback Equalization Sub Threshold Logic for Digital Logic Circuit

Shivaraj I Math
Department of studies in VLSI and Embedded System, VTU Belagavi, India
mshivaraj59@gmail.com

Abstract— In embedded application ultra-low power sub threshold logic is prominently used with limited energy budgets. When we operate digital logic circuits in sub threshold region it consumes less power. In this paper we propose 4-bit adder design in cadence with technology of 180nm and this 4-bit adder designed with logic of tuneable adaptive feedback equalizer. Using this logic we mitigate the power consumption and reduce the delay. We present detailed operation 4-bit adder with tuneable adaptive feedback equalizer logic by giving minimum power supply voltage we observe the power dissipation and delay of the circuit. In conventional 4-bit adder the delay is 71.8% and in proposed 4-bit adder the delay is 37.5% we reduced delay from 71.8% to 37.5%.

Keywords— 4-bit adder, Feedback equalizer, leakage energy component, subthreshold

I. INTRODUCTION

Now days subthreshold CMOS digital circuits are more popular in energy power application. The main idea is to scale down the power supply by scaling down the power supply voltage we can reduce the dynamic energy and also reduces the leakage current. The usage of feedback equalizer circuit for lowering the energy consumed by the digital circuit. In this tunable feedback equalizer logic digital circuits are operating in subthreshold region and this logic is used to reduce the power and delay of the digital circuit.

There are many several techniques have been proposed to design robust ultra_low power sub_threshold circuits detailed analysis on the timing variability and the meta_stability of the flipflops designed in the sub_threshold region[1]. In some digital circuits boost the drain current of the transistors using minimum_sized devices[2]. The a current reference circuit to design a regulator for voltage and that provide a supply voltage that makes the propagation delay of the sub_threshold[3]. suppress leakage in the sub_threshold circuits. Error detection and correction techniques have been most commonly used to design[4]. tunable replica circuit and error-detection sequentials to monitor dynamic variation guardbands and critical path delays mitigate for maximum throughput in the above threshold region[5].

The paper is organized as follows in section[I] we discussed the related work in the design of subthreshold circuits. In section [II] we explain about the feedback equalizer logic. A detailed operation of 4-bit adder with feedback equalizer logic in section [III]. In section [IV] conclusion.

II. ADAPTIVE EQUALIZED FLIP-FLOP VERSUS CONVENTIONAL FLIP- FLOP

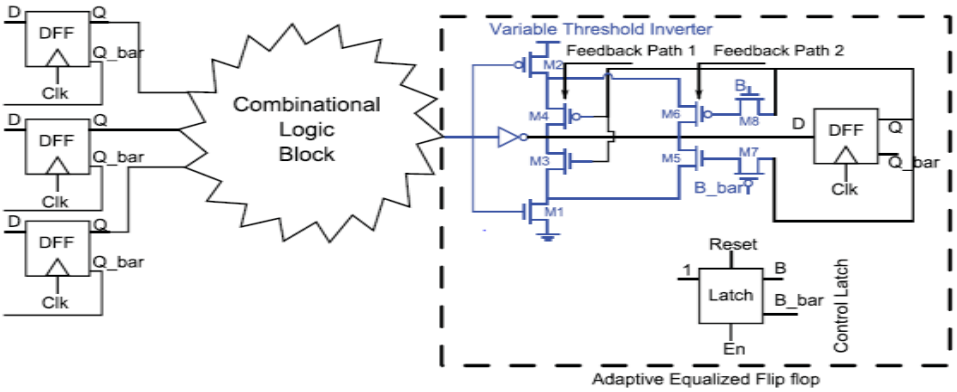


Fig 1 Adaptive feedback equalizer circuit with multiple feedback(e-logic)

We first need to known the use of the adaptive feedback equalizer circuit and how it will help in the design of an adaptive equalized flip-flop (E-flip-flop) and then we provide a detailed comparison between Equalized flipflop with the conventional flip-flop in terms of setup time, area, and performance. We propose the variable threshold inverter as an adaptive feedback equalizer along with the classic master_slave positive edge_triggered flipflop design an adaptive E-flip-flop. The adaptive feedback equalizer circuit has two feed forward transistors (M1 and M2 in Fig. 3.1) and four control transistors (M3 and M4 transistor for feedback path one that is always ON and M5 and M6 transistors for feedback path two that can be operate conditionally switched ON post fabrication in Fig.1) that provide extra pull-up/pull-down paths for the circuit in addition to the pull-up/pull-down path in the static inverter for the FlipFlop Data input capacitance. The extra pull-up/pull-down paths are enabled based on the output of the critical path in the combinational logic changes in the circuit. The control transistors M5 and M6 are enabled/disabled through transistor switches (M7 and M8 transistors) and this are controlled by an asynchronous control latch. The initial value of the static control latch is reset to 0 during chip boot up. After boot up, if there is requirement of square pulse is sent to the Enble terminal and to set the output of the latch from 0 to 1 to switch ON M7 and M8 transistors, which enables the feedback path 2. The adaptive E-flip_flop effectively modified by the switching threshold of the static inverter in the adaptive feedback equalizer and it is based on the output of flipflop in the previous cycle. If the flipflop output is 0 for the previous cycle, static inverter of the switching threshold is lowered, because of this, it speeds up the transition state of the flipflop input from 0 to 1. Similarly if the previous output of flipflop is 1, then switching threshold is increased, which speeds up the transition state to 0. Effectively, the feedback equalizer circuit adjusts the switching threshold and also it facilitates faster high-to-low and low-to-high transitions state of the flipflop input. Moreover, the small value of input capacitance of the feedback equalizer reduces the switching time of the combinational logic block for the last gate in the circuit.

The adaptive feedback equalizer circuit can reduce the propagation delay of the critical path because of this; it significantly reduces the switching time of the last gate in the combinational logic circuit.

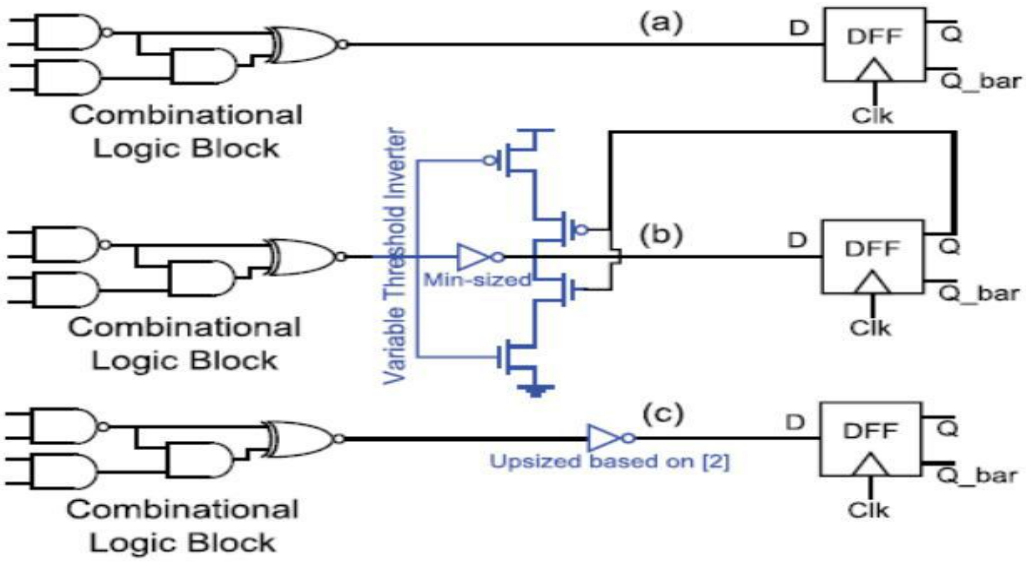


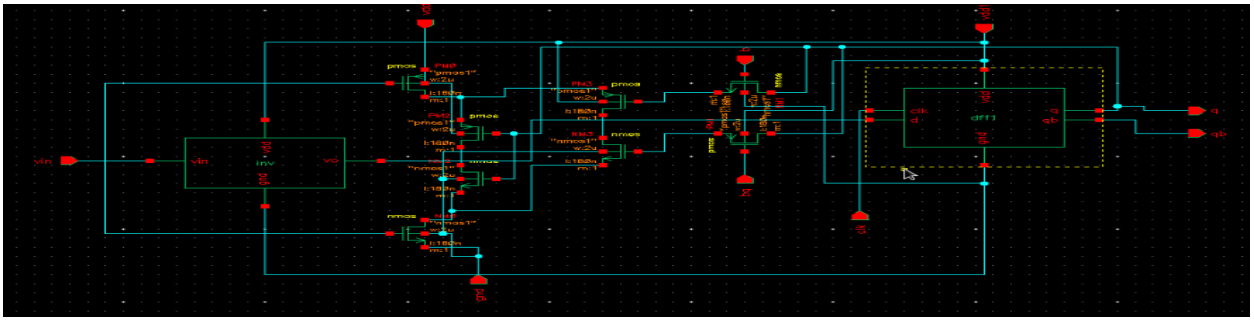
Fig 2 (1)Original Non-Equalized Design (2) Equalized Design (3) Buffer Inserted Non-Equalized Design

III.PERFORMACE ANALYSIS OF PROPOSED MODIFIED FULL ADDER

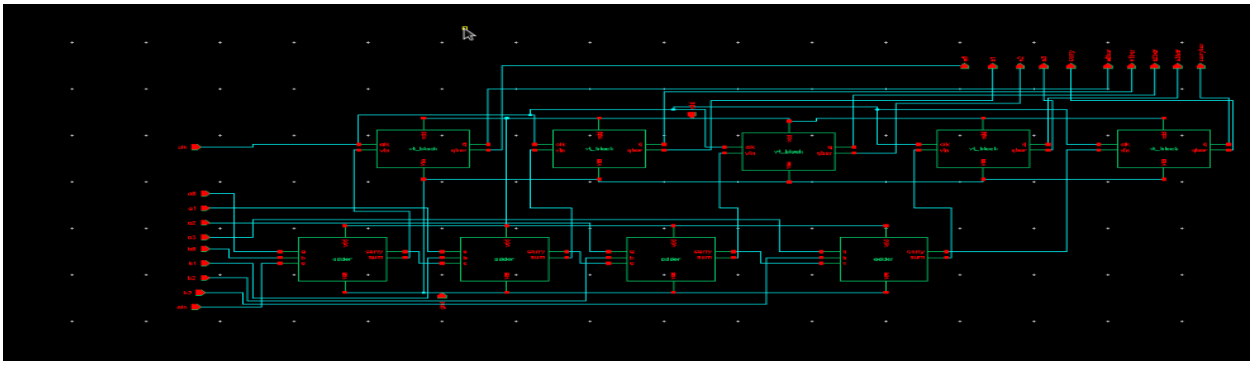
The proposed modified Full adder structure's performance is verified against the existing Full adder structure by designing along with Adaptive feedback equalizer. We have used 180nm CMOS process technology model library from Cadence, Power supply VDD is varies for all simulations. Circuits are simulated in Cadence simulator. Show the plot of output voltage from the Adaptive feedback equalizer.

The energy delay product is less than the existing full adder circuit and also consumes less power as compared to the existing full adder. As the supply voltage is reduced the power dissipation is also reduced according to the supply voltage. The power dissipation for our design is shown in the below table1.And also it reduces the critical delay.

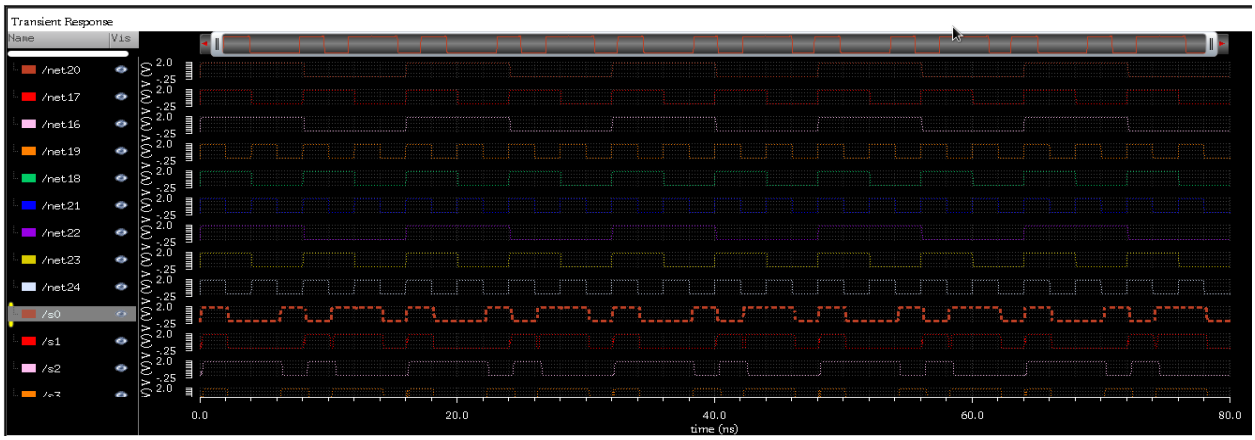
Proposed Adaptive feedback equalizer circuit Fig(3)



Appling this Adaptive feedback equalizer to the adder Fig(4)



Output Waveform of full adder fig(5)



With different power supply we observe the power dissipation

Result Table1

Technology (nm)	Logic Style	Min_Energy Supply Voltage (mV)	Power Dissipation
180	E-Logic	380	1.75u
180	E-Logic	350	1.34u
180	E-Logic	300	423.6n

IV. CONCLUSIONS

Proposed 4-bit adder with adaptive feedback equalizer logic to reduce the usage of supply voltage. the digital cmos circuit operates in sub_threshold regime. We can adjusting the switching thresholds of the transistor based on the sampled outputs, the feedback equalization circuit which helps us in faster switching of the logic gate outputs and provides the opportunity to reduce the leakage current in weak inversion region that is sub_threshold region. We also implemented a non-equalized flipflop and an equalized flipflop design, by using this technique we design an 4-bit full adder in cadance 180 *nm* process using CMOS technology and try to manage to reduce the propagation delay of the critical path of the sub-threshold logic and leakage energy, leading to 34% decrease in energy-delay product of the conventional non-equalized design at minimum energy supply voltage.

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