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RESEARCH ARTICLE

VLSI Architecture for Implementing Kaiser Bessel Window Function Using Expanded Hyperbolic CORDIC Algorithm

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Abstract - Windowing techniques have been widely used for preprocessing of samples before fast Fourier transform (FFT) in real time spectral analysis to minimize spectral leakage and picket fence effect. Among all popular window functions, Kaiser-Bessel window is an obvious choice for its better spectral characteristics. In this paper, CORDIC (CO-ordinate Rotation Digital Computer) based VLSI architecture for implementing Kaiser-Bessel window has been proposed for real time applications. The parallel pipelined technique has been adopted for the present design to ensure high throughput. Various architectural design and implementation issues have been discussed. The physical synthesis for ASIC implementation of proposed architecture using Synopsys design compiler(Design Vision) and commercially available 0.18 μm CMOS yields the core area of 52 mm2 and worst case dynamic power of 890 mW at an operating frequency and voltage of 400 MHz and 1.8 V respectively.

Keywords: VLSI architecture, Kaiser-Bessel windowing function, CORDIC

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