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RESEARCH ARTICLE

VLSI Implementation and Analysis of Parallel Adders for Low Power Applications

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Abstract— ***Carry select adder (CSLA) is known to be the fastest adder among the conventional adder structures. Due to the rapidly growing mobile industry not only the faster arithmetic unit but also less area and low power arithmetic units are needed. The modified CSLA architecture has developed using Binary to Excess-1 converter (BEC). The efficient CSLA architecture has developed using D latch. In this paper an analysis has been made between Regular and Conventional CSLA adders like modified, Efficient CSLA. Designs were developed using structural VHDL and synthesized in Altera Quartus II with reference to FPGA device EP2C35F672C6. Experimental results are compared in-terms of area, power, delay and PDP. Results shows that modified carry select adders are better in area and power consumption.***

Keywords— ***CSLA, Adders, Low Power, VHDL, VLSI***

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