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RESEARCH ARTICLE

POWER AND AREA EFFICIENT DESIGN OF COUNTER FOR LOW POWER VLSI SYSTEM

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Abstract— The objective of this project is to design the sequential circuit's using different sequential circuit components and analyze the different characteristics such as power conception and area occupation etc. by sequential circuit designed using microwind.

I. MICROWIND

ABOUT DSCH:

The DSCH2 program is a logic editor and simulator. DSCH2 is used to validate the architecture of the logic circuit before the microelectronics design is started. DSCH2 provides a user friendly environment for hierarchical logic design, and simulation with delay analysis, which allows the design and validation of complex logic structures. A key innovative feature is the possibility to estimate the power consumption of the circuit. Some techniques for low power design are described in the manual.

ABOUT MICROWIND:

The MICROWIND2 program allows the student to design and simulate an integrated circuit at physical description level. The package contains a library of common logic and analog ICs to view and simulate. MICROWIND2 includes all the commands for a mask editor as well as original tools never gathered before in a single module (2D and 3D process view, VERILOG compiler, tutorial on MOS devices). You can gain access to *Circuit Simulation* by pressing one single key. The electric extraction of your circuit is automatically performance and the analog simulator produces voltage and current curves immediately.

II. VLSI: VERY LARGE SCALE INTEGRATION

Electronics is characterized by reliability, low power dissipation, extremely low weight and volume, low cost, high degree of sophistication and complexity. Vacuum tubes were used for electronic circuits during the first half of the 20th century. When electronic components started emerging a new dimension, transistors replaced vacuum tubes in 1948 which were superseded by IC demonstrated by Er.jalkKilby of Texas instruments in 1958. VLSI the small GIANT, was initially formulated in 1975 which now occupies the shelves of manufacturers of all microelectronic equipment's. The work of both jalky and Robert noyce of fair child developed the field of VLSI.

VLSI (very large-scale integration) is the current level of computer microchip miniaturization and refers to microchips containing in the hundreds of thousands of transistor s. LSI (large-scale integration) meant microchips containing thousands of transistors. Earlier, MSI (medium-scale integration) meant a microchip containing hundreds of transistors and SSI (small-scale integration) meant transistors in the tens.

CMOS (complementary metal-oxide semiconductor):

CMOS (complementary metal-oxide semiconductor) is the semiconductor technology used in the transistors that are manufactured into most of today's computer microchips. Semiconductors are made of silicon and germanium, materials which "sort of" conduct electricity, but not enthusiastically. Areas of these materials that are "doped" by adding impurities become full-scale conductors of either extra electrons with a negative charge (N-type transistors) or of positive charge carriers (P-type transistors). In CMOS technology, both kinds of transistors are used in a complementary way to form a current gate that forms an effective means of electrical control. CMOS transistors use almost no power when not needed. As the current direction changes more rapidly, however, the transistors become hot. This characteristic tends to limit the speed at which microprocessors can operate.

FREQENCY IMPROVES:

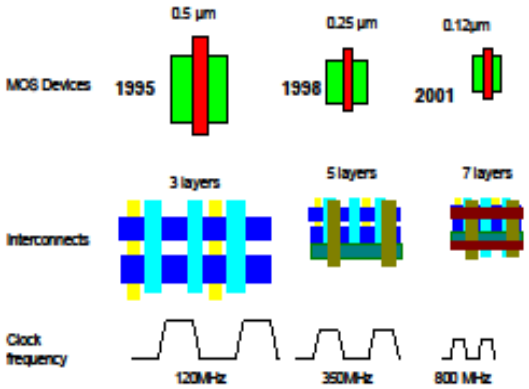


Figure illustrates the main improvements in terms of feature size reduction for MOS device increased of metal interconnects to link MOS together within the chip consequently; the clock frequency of the chip has never stopped increasing with an expected 800MHz in 2011. The microwind using 0.8 & 0.25 micrometers technologies.

This chapter presents the CMOS transistor, its layout, static characteristics and dynamic characteristics. The vertical aspect of the device and the three dimensional sketch of the fabrication are also described.

The MOS as a switch

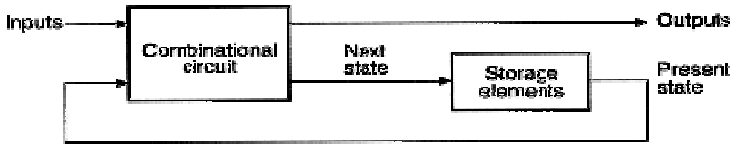
The MOS transistor is basically a switch. When used in logic cell design, it can be *on* or *off*. When on, a current can flow between drain and source. When off, no current flow between drain and source. The MOS is turned on or off depending on the gate voltage. In CMOS technology, both n-channel (or NMOS) and P channel

MOS (or P MOS) devices exist. The NMOS and PMOS symbols are reported below. The n-channel MOS is built using poly silicon as the gate material and N+ diffusion to build the source and drain. The P channel MOS is built using poly silicon as the gate material and P+ diffusion to build the source and drain. The symbols for the ground voltage source (0 or VSS) and the supply (1 or VDD) are also reported.

SEQUENTIAL CIRCUITS:

Combinational logic is useful for interesting operations like decoding, encoding, addition and subtraction. However, sequence of operations is cumbersome to handle using combinational logic methods.

Combinatorial logic interconnected with storage elements gives rise to sequential circuits. In combinational circuit, the output is only a function of all inputs and given any combination of inputs, it is always possible to predict the output. In sequential circuit, the output is not only a function inputs but history of the input changes.

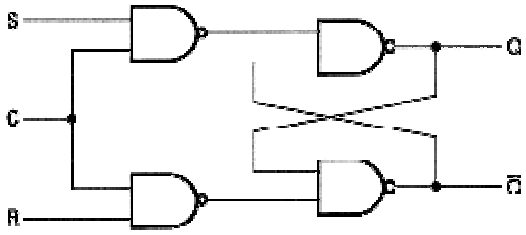


FLIP FLOP:

It is a storage element based on gated latch principle, which can have its output changed only on the edge of the controlling clock signal. The combination of number of flip flops makes a sequential circuit. The Flip-Flop remains locked on an output of either 0 or 1 until it is given some sequence of inputs, in which case its output will change.

SR Flip Flop:

An alternate form of the *SR latch*, in this case the *set* and *reset* signals active low, can be constructed using NAND gates as follows .One way to prevent the system from becoming unstable is by means of *gating* the *set* and *reset* inputs using a *control* input.

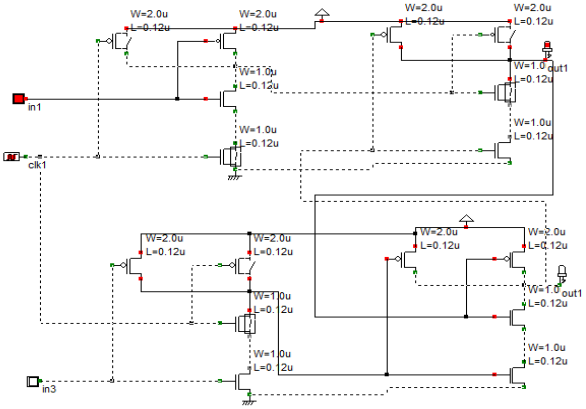


(a) Logic diagram

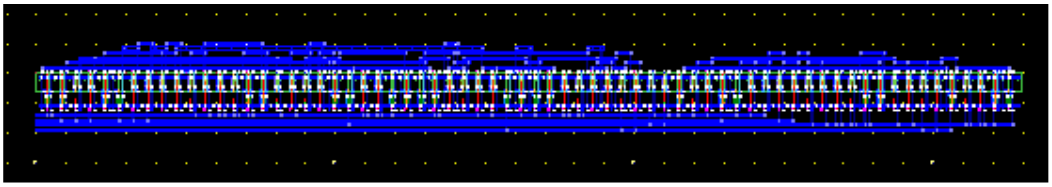
C	S	R	Next state of Q
0	X	X	No change
1	0	0	No change
1	0	1	Q = 0; Reset state
1	1	0	Q = 1; Set state
1	1	1	Undefined

(b) Function table

Design SR flip flop: (using CMOS)

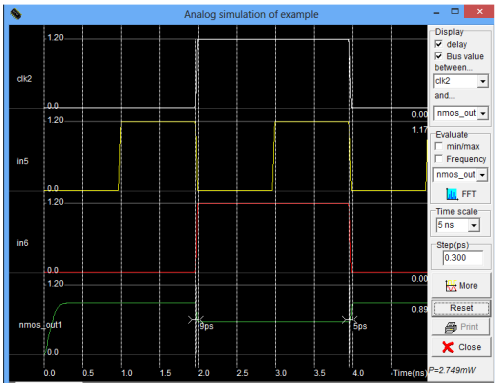


III. LAYOUT MODEL



The SR flip flops are used 16cmos gates . Area occupation of 879.1um power efficient of 2.749mw

TIMING DIAGRAM:



SR flip flop takes high power and area than jk flip flop.so design J-K flip flop.

J-K flip flop:

The J-K flip-flop has two outputs, one being the conjugate of the other. The J-K flip-flop is constructed NAND and NOT gates as shown. The J-K flip-flop outputs reflect the J and K inputs upon the pulse of the clock, but remain locked until then except in the case where J=K=1 where the outputs simply flip upon a pulse.

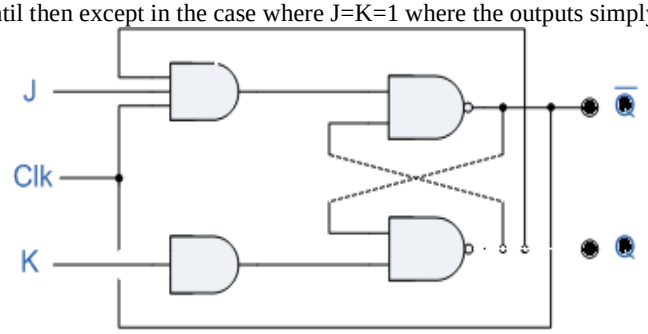
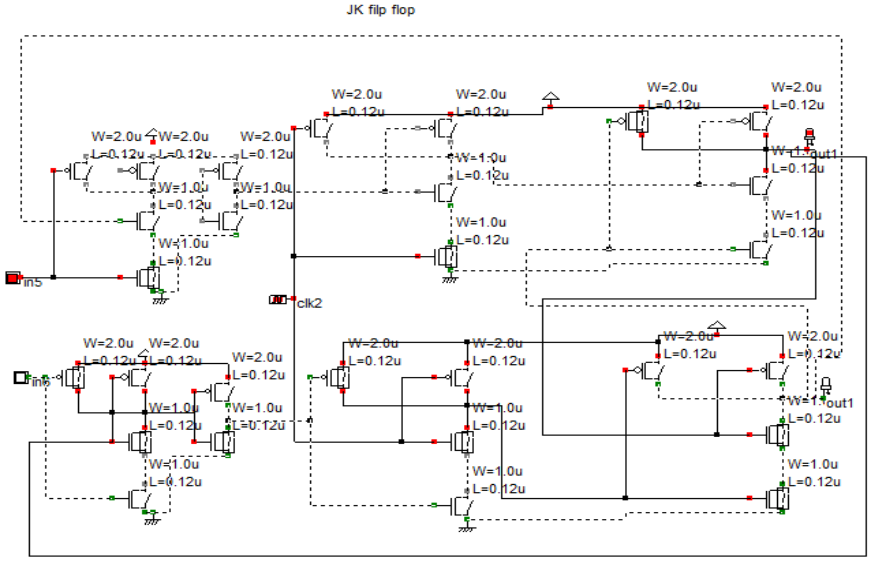


Figure 1

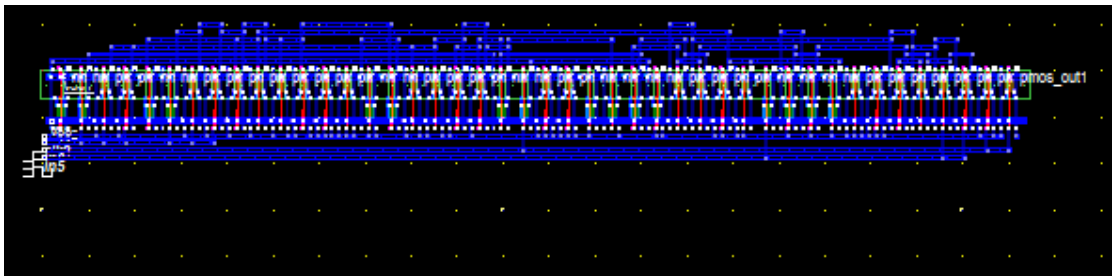
The figure 1 and figure 2 are the work at the JK flip flop. The both are the same work but the figure 2 form by the CMOS gates. I this Flip flop the 24 CMOS gates are used.

ANALOG SIMULATION

The power conception of the CMOS jk flip flop is um. The area occupation is 572.2um.

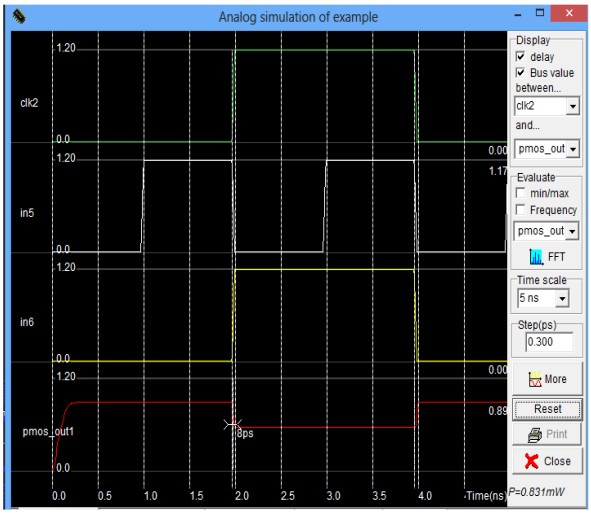


Layout model:



The jk flip flops are used 28cmos gates . Area occupation of 572.2um power efficient of 0.082mw.

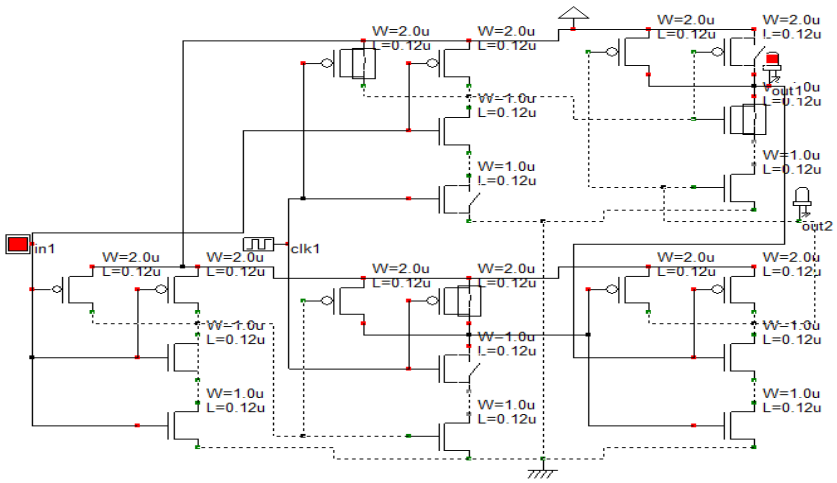
Power analysis:



SR and J-k flip flops both are takes high power and area occupation compare than D flip flop. so design D flip flop.

IV. **D FLIP FLOP**

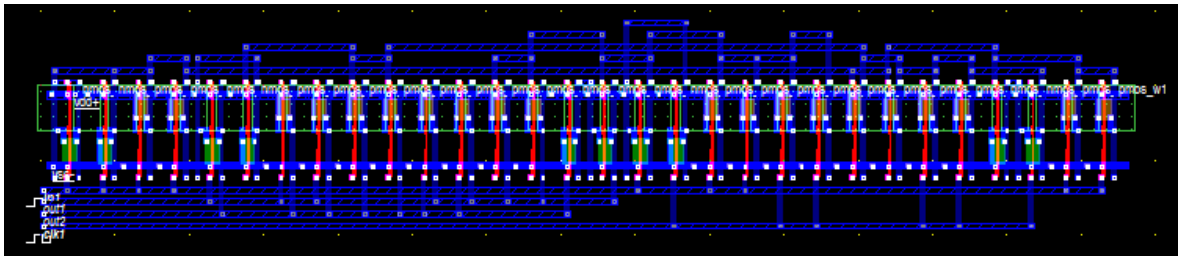
The D flip flop I's means differential amplifier. The work manner is same for the jk flip flop .only difference is the d flip flop are used in the NOT gate. The area and power conception and area will be reduced so the D flip flop is used.



The above figure 1 is the cmos based D flip flop. In the D flip flop also same as the JK flip flop but in this flip flop NOT gate will be used.

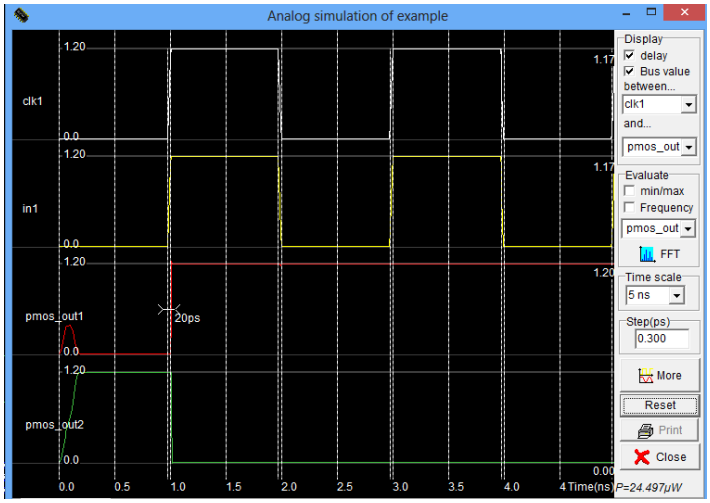
It will perform the D flip flop operation. The 20 CMOS gates are used. The area occupation is 372.0um.power conception is In this area will be reduced the modified D flip flop are used,

Layout model:



It will perform the D flip flop operation. The 20 CMOS gates are used. the area occupation of area is 372.2um and power consumption is 24.497uw

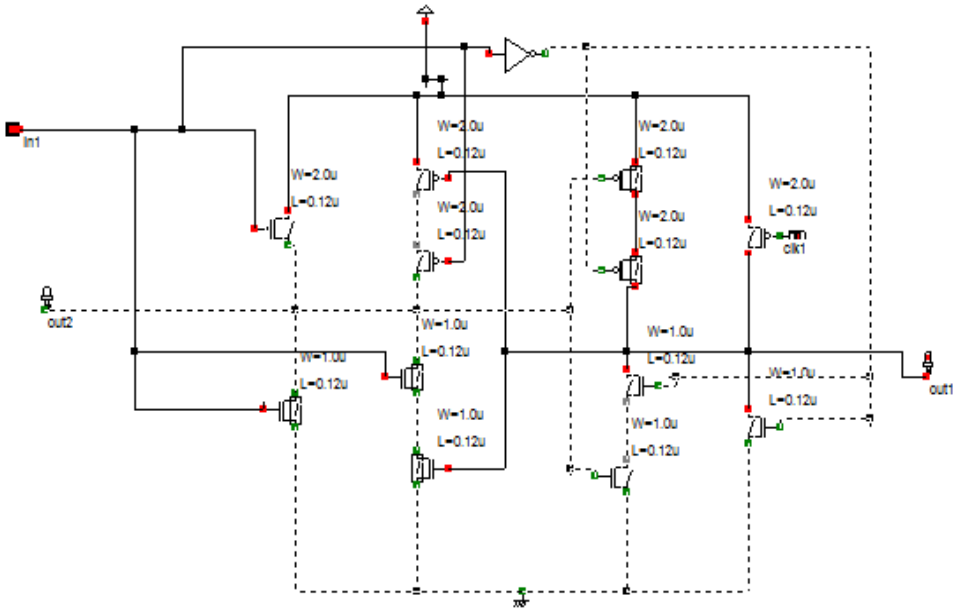
POWER ANALYSIS:



V. MODIFIED D FLIP FLOP

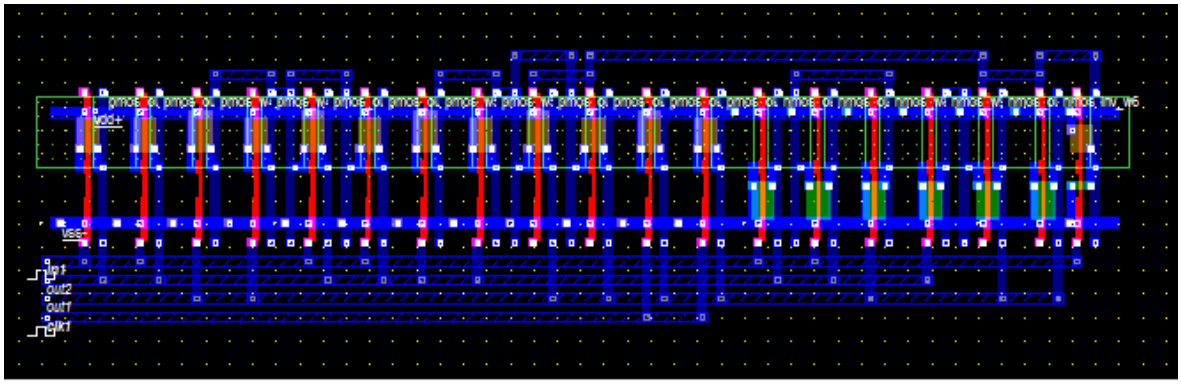
The above figure is the modified cmos based D flip flop. In the D flip flop also same as the JK flip flop but in this flip flop NOT gate will be used.

It will perform the D flip flop operation. The 12 CMOS gates are used.

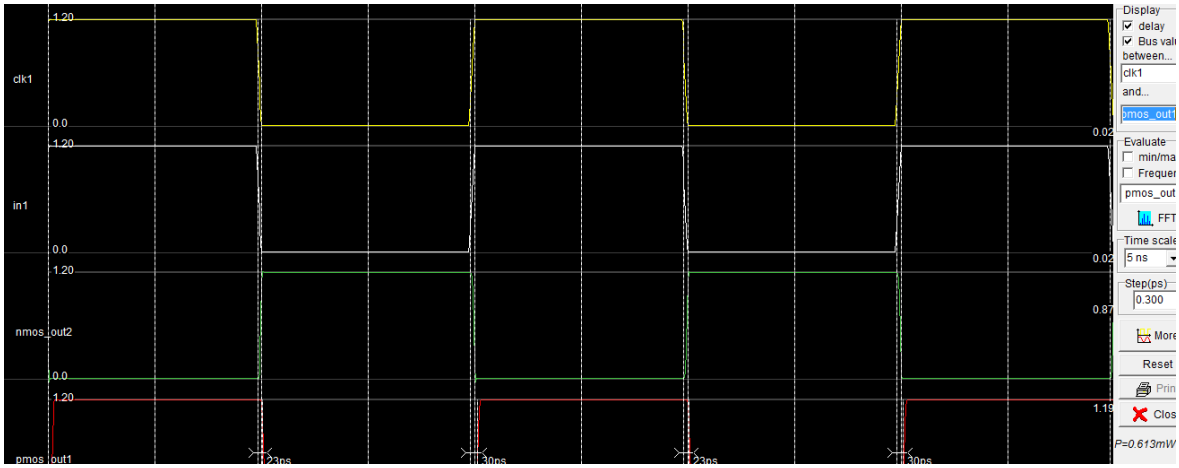


In this area will be reduced the modified D flip flop are used,

LAYOUT MODEL:



POWER ANALYSIS:



The modified area occupation is 194.16um^ 2. Power conception is 0.613mw.

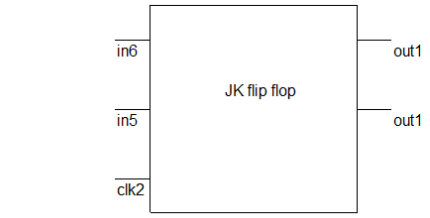
VI. PARAMETER COMPARISON

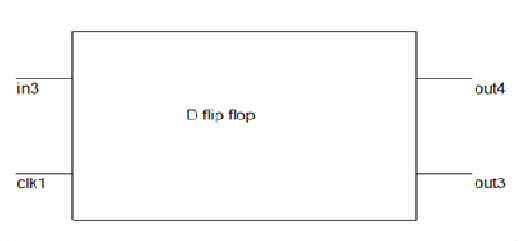
FLIP FLOP	NO. OF TRANSISTORS USED	AREA in um^2	POWER CONCEPTION
SR FF	16	879.1	2.749mw
JK FF	28	572.2	.082 mw
D FF	20	372.0	24.497uw
Modified d ff	10	194.16	0.613mw

The above comparisons the D flip flop all parameters lower than J-K flip flop .so this D flip flop will be used to design the counters.

VII. CONVERT INTO BLOCKS

The above cmos based flip flop are converted into the block option available in DSCH software.it operates at same working. The blocks are





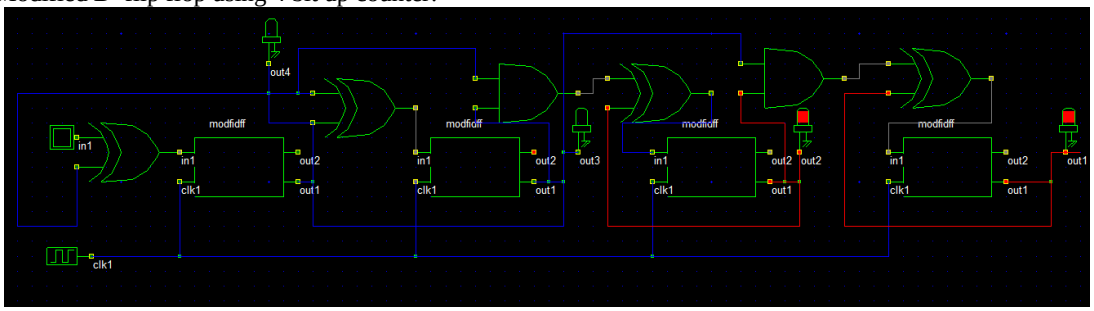
VIII. COUNTERS

Counters are one of the many applications of sequential logic that has a widespread use from simple digital alarm clocks to computer memory pointers. A counter is a collection of flip flops, each representing a digit in a binary number representation (which means each bit, depending on position, means a different number).

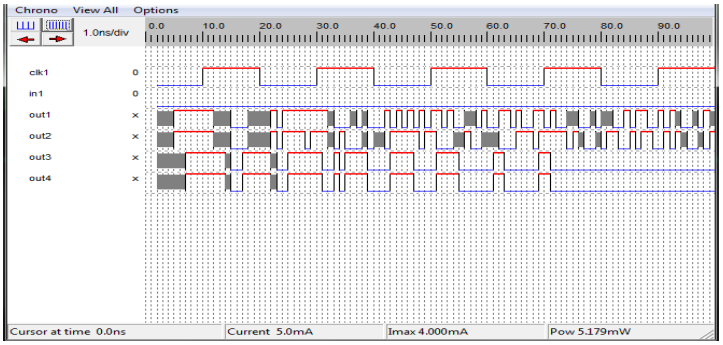
One of easier ways to build a circuit is to make a flip flop that controls the activation or switching of the second, and so on. This type of counter is called a ripple counter, since the switching signal propagates from one flip flop to the next as in a wave.

Counter is a device which generates an n- bit output sequence of a maximum of 2^n states in synchronism with a clock. It consists of an array of flip flop which operates in toggle mode ie., complements it previous output if toggle input is 1. Binary counters generates all the possible 2^n states at the output, e.g. a 4 bit counter generate all the 16 states 0000,0001,0010,…….1111 in successive clock cycles and repeats thereafter.

Modified D flip flop using 4 bit up counter:



Timing diagram



The above figure is modified D flip flop based up counter. The output of the counter is 0000, 0001, 0010 ,…… 1111 it's operates on the continues sequence .The area of the counter is **632.5um^2.** The power conception is **0.902mW.**

VERILOG CODE:

D flip flop:

```
module d ff 1( clk1,in1,out1,out2);
 input clk1,in1;
 output out1,out2;
 nmos #(1) nmos(w1,w1,in1); // 1.0u 0.12u
 nmos #(1) nmos(w1,vss,in1); // 1.0u 0.12u
 pmos #(1) pmos(w1,vdd,in1); // 2.0u 0.12u
 nmos #(1) nmos(out2,w3,out1); // 1.0u 0.12u
 nmos #(1) nmos(w3,vss,w6); // 1.0u 0.12u
 pmos #(1) pmos(out2,vdd,out1); // 2.0u 0.12u
 pmos #(1) pmos(out2,vdd,w6); // 2.0u 0.12u
 pmos #(1) pmos(out1,vdd,out2); // 2.0u 0.12u
 pmos #(1) pmos(out1,vdd,w7); // 2.0u 0.12u
 nmos #(1) nmos(w8,vss,out2); // 1.0u 0.12u
 nmos #(1) nmos(out1,w8,w7); // 1.0u 0.12u
 nmos #(1) nmos(w7,w9,in1); // 1.0u 0.12u
 nmos #(1) nmos(w9,vss,clk1); // 1.0u 0.12u
 pmos #(1) pmos(w7,vdd,in1); // 2.0u 0.12u
 pmos #(1) pmos(w7,vdd,clk1); // 2.0u 0.12u
 pmos #(1) pmos(w6,vdd,w1); // 2.0u 0.12u
 pmos #(1) pmos(w6,vdd,clk1); // 2.0u 0.12u
 nmos #(1) nmos(w11,vss,w1); // 1.0u 0.12u
 nmos #(1) nmos(w6,w11,clk1); // 1.0u 0.12u
 pmos #(1) pmos(w1,vdd,in1); // 2.0u 0.12u
endmodule
```

MODIFIED D FLIP FLOP:

```
module mod dff( in1,out1,out3);
 input in1;
 output out1,out3;
 nmos #(1) nmos(w2,vss,out3); // 1.0u 0.12u
 nmos #(1) nmos(out3,vss,in1); // 1.0u 0.12u
 pmos #(1) pmos(w5,vdd,out1); // 2.0u 0.12u
 pmos #(1) pmos(out3,w5,in1); // 2.0u 0.12u
 nmos #(1) nmos(out3,w6,in1); // 1.0u 0.12u
 nmos #(1) nmos(w6,vss,out1); // 1.0u 0.12u
 pmos #(1) pmos(out3,vdd,in1); // 2.0u 0.12u
 pmos #(1) pmos(w7,vdd,out3); // 2.0u 0.12u
 pmos #(1) pmos(out1,w7,w8); // 2.0u 0.12u
 nmos #(1) nmos(out1,w2,w8); // 1.0u 0.12u
 not #(1) inv(w8,in1);
 pmos #(1) pmos(out1,vdd,w9); // 2.0u 0.12u
 nmos #(1) nmos(out1,vss,w8); // 1.0u 0.12u
endmodule
```

IX. ADVANTAGES

1. The main advantages of this soft tool are, it will reduce program written and also it's a program generator.
2. The user knows what operation will perform the components in the circuits.
3. The user first implement the soft tool and it will run after the user can invest cost to the materials.
4. To directly measure the parameters such as power conception, area, temperature, etc.

X. CONCLUSION

Thus the sequential circuit is designed with low power and area conception. The obtained area and power conception is **632.5um^2, 0.902mW.**

