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RESEARCH ARTICLE



A Novel Design of Reversible Universal Shift Register

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*Abstract: Reversible logic gates provide power optimization which can be used in low power CMOS design, optical computing, quantum computing and nanotechnology. This paper propose a new 4*4 reversible RR gate that works as a reversible 4:1 multiplexer and has a reduced quantum cost. A novel design of Reversible Universal shift register using RR gates with reduced delay and quantum cost is proposed.*

Keywords: Flip Flop, Multiplexer, Reversible logic Gate, Garbage Output, Quantum Cost

1. INTRODUCTION

The shift Register is one of the most extensively used functional Device in digital system. Shift Register Consist of Group of Flip-Flops connected together so that information bits can be shifted one position to either right or left depending on the design device.

Reversible circuits are of high interest in the field of low power CMOS design, optical computing, quantum computing and nano-technology .With increasing complexity of CMOS VLSI circuits, Power dissipation is the main area of concern in VLSI design. Rolf Launder [1] shown that for conventional irreversible logic computation each bit of information lost generates $KT \ln 2$ joules of heat energy. Where K is Boltzmann constant and T is absolute temperature. Later, Charles H. Bennet [2]

showed that Ktln2 joules of energy are not loosed in reversible computations. Reversible logic circuits are designed by reversible gates. Reversible logic has extensive applications in future technologies such as nano-technology, Quantum computing, Cellular automata etc. The important cosmetics in reversible logic circuits are the quantum cost, the delay, and the number of garbage outputs. We modified existing Fredkin gate (FRG) in two ways one is modified FRG1 To design efficient 4-1 Multiplexer and modified FRG2 to design D flip-flop.

1.1. Quantum Cost

The quantum cost of a 1*1 Gate is Zero and the any 2*2 Gate is one. The Quantum cost of Reversible can be calculated by counting the numbers of NOT, Controlled V and CNOT Gates Required in its implementation. The quantum cost of a 2*2 Feynman gate is 1 while the quantum cost of 3*3 Fredkin and Peres gate is 5 and 4 respectively.

1.2. Garbage outputs

Garbage output is the unwanted or unread outputs which are needed to maintain the reversibility of the reversible gate (circuits). Number of garbage outputs for a particular reversible gate is not fixed, but any output that is not used in a circuit in which the gate is used is labeled garbage outputs.

2. BASIC REVERSIBLE GATES

Reversible Gate is a k-input, k-output (k*k) circuit that produces a unique output pattern for each input pattern. There are several 2*2 , 3*3 and 4*4 reversible gates such as the Feynman gate, Fredkin gate, Toffoli gate and RR gate. A reversible circuit should be design using minimum number of reversible logic gates.

2.1 FEYNMAN GATE (FG)

The Feynman gate (FG) is a 2-input 2-output reversible gate having the mapping (A, B) to (P=A, Q = A⊕B) where A, B are the inputs and P, Q are the outputs respectively as shown in fig. 1. The Feynman gates are used for fan-out operations. The quantum cost of Feynman gate is 1.

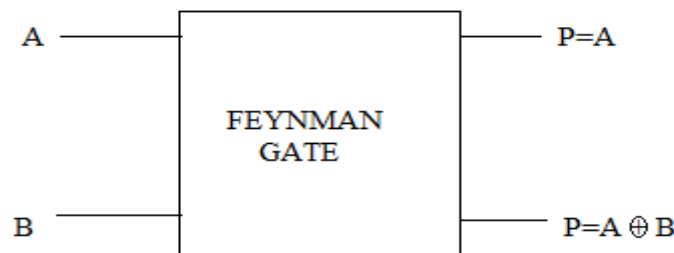


Figure 1. Feynman Gate

2.2 FREDKIN GATE (FRG)

A Fredkin gate (FG) is a 3*3 conservative reversible gate having the mapping (A, B, C) to (P = A, Q = A'B ⊕ AC, R = AB ⊕ A'C), where A, B, C are the inputs and P, Q, R are the outputs respectively. The Fredkin gate is shown in fig. 2. The quantum cost of Fredkin gate is 5.

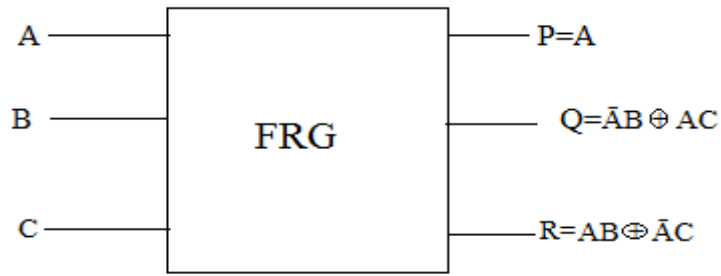


Figure 2. Fredkin Gate

2.3 TOFFOLI GATE (TG)

Toffoli Gate is a 3*3 two through reversible gate as shown in fig. 3. Two through means two of its outputs are the same as inputs with the mapping (A, B, C) to (P = A, Q = B, , R = A · B ⊕ C), where A, B, C are inputs and P, Q, R are outputs respectively. The quantum cost of Toffoli gate is 4.

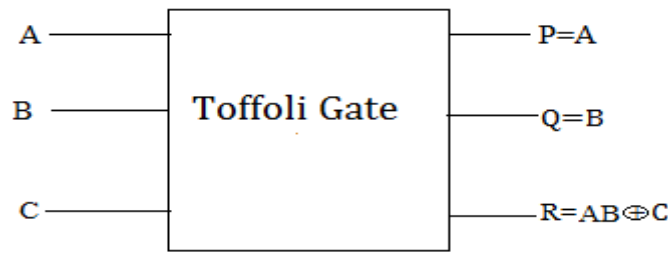


Figure 3. Toffoli Gate

3. PROPOSED 4*4 RR REVERSIBLE GATE

This paper present a new 4*4 parity preserving reversible gate, RR Gate is shown in figure. The gate is one through, which means one of the input variables is also output. This is already Verified by comparing the input parity $A \oplus B \oplus C \oplus D$ to the output parity $P \oplus Q \oplus R \oplus S$. The Quantum cost of RR gate is calculated to be equal to 4 and that of Fredkin gate used in existing designs [4]

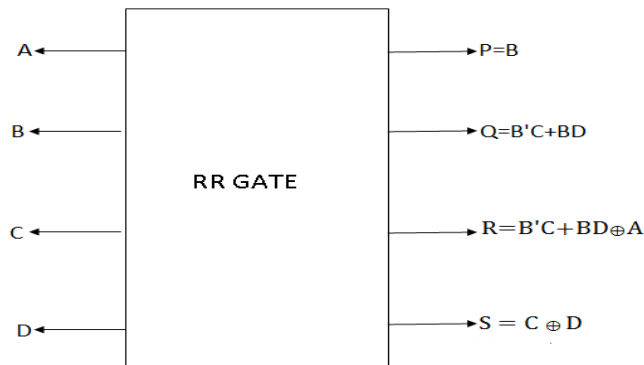


Figure 4. RR Gate

4. PROPOSED DESIGN OF UNIVERSAL SHIFT REGISTER

The universal shift register store binary data and its data can be shifted left or right when a clock signal is applied. All modes of operation such as SISO (serial-in-serial output), SIPO (serial-in-parallel output), PISO (parallel-in-serial output) and PIPO (parallel-in-parallel output) can also be performed upon the occurrence of clock. Fig. 5 shows the propose universal shift register. Thus, serial data (SIR during right shift and SIL during left shift) or parallel data can be loaded into shift register. The values of the select lines determine the operation to be performed as given in table 1.

The existing design of Reversible Universal Shift Register in reference [11] is basically built from basic cells comprising of DFF, Feynman gate (FG) and Fredkin gates. In the existing design fanout circuits are not used for any of the signals.

Table 1. Operation of Universal Shift Register

S1	S0	Operation
0	0	No Change
0	1	Right Shift
1	0	Left Shift
1	1	Parallel Load

The four multiplexers have two common selection inputs S1 and S0. Input 0 in each multiplexer is selected when S1S0 = 00, input 1 is selected when S1S0 = 01 and similarly for other two inputs.

The proposed design of Universal Shift Register shown in fig. 5 consist of flip-flops blocks that can make use of the design of Master slave D flip-flop, D flip-flop with synchronous or asynchronous set/reset and 4:1 Multiplexer design.

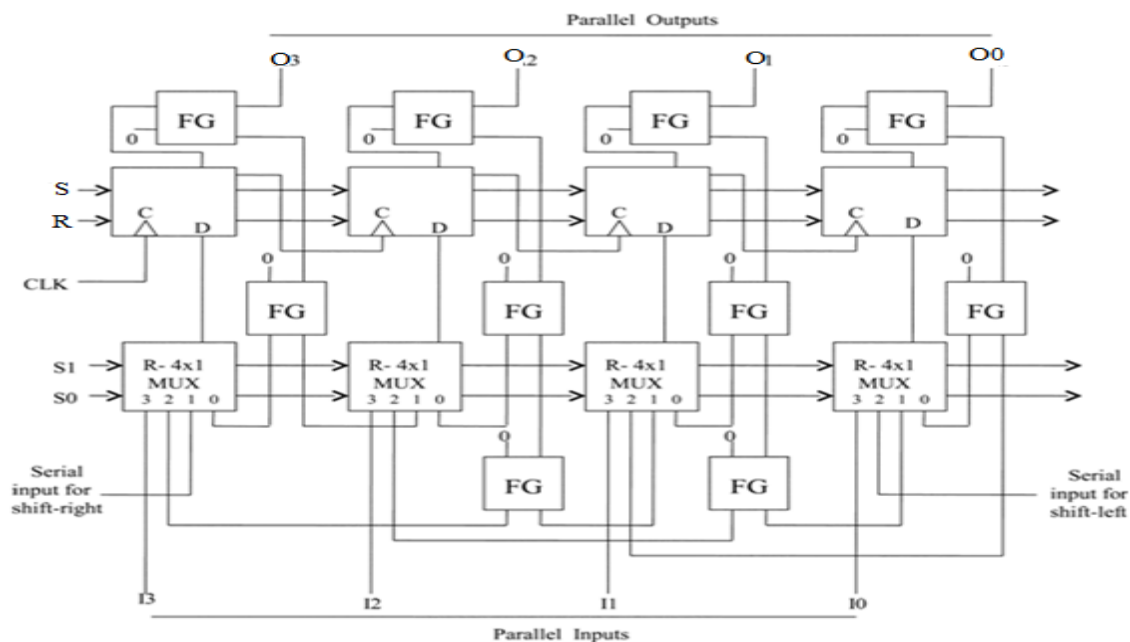


Figure 5. Proposed Design of Reversible Universal Shift Register

5. PERFORMANCE EVALUATION

The proposed Reversible Universal Shift Register has Quantum cost 110, delay 110 and Garbage output is 36. The proposed design of Reversible Universal Shift Register achieves improvement ratios of 23%, 23% and 10% in terms of quantum cost, delay and garbage outputs compared to the design presented in existing [10]. The improvement ratios compared to design presented in existing [11] are 8% , 8% and 0% in terms of quantum cost and delay. The results are shown in table 2.

Table 2. Comparison of Reversible Universal Shift Register

Design of Universal Shift Register	Quantum cost	Delay	Garbage Outputs
Proposed	110	110	36
Existing[09]	144	144	40
Existing[10]	120	120	36
Improvement (%) w.r.t [9]	23	23	10
Improvements (%) w.r.t[10]	8	8	0

6. IMPLEMENTATION AND RESULT

The proposed design was functionally verified and results are verified. The functional design was verified in Xilinx. The output waveform of reversible universal shift register is shown in fig. 6.

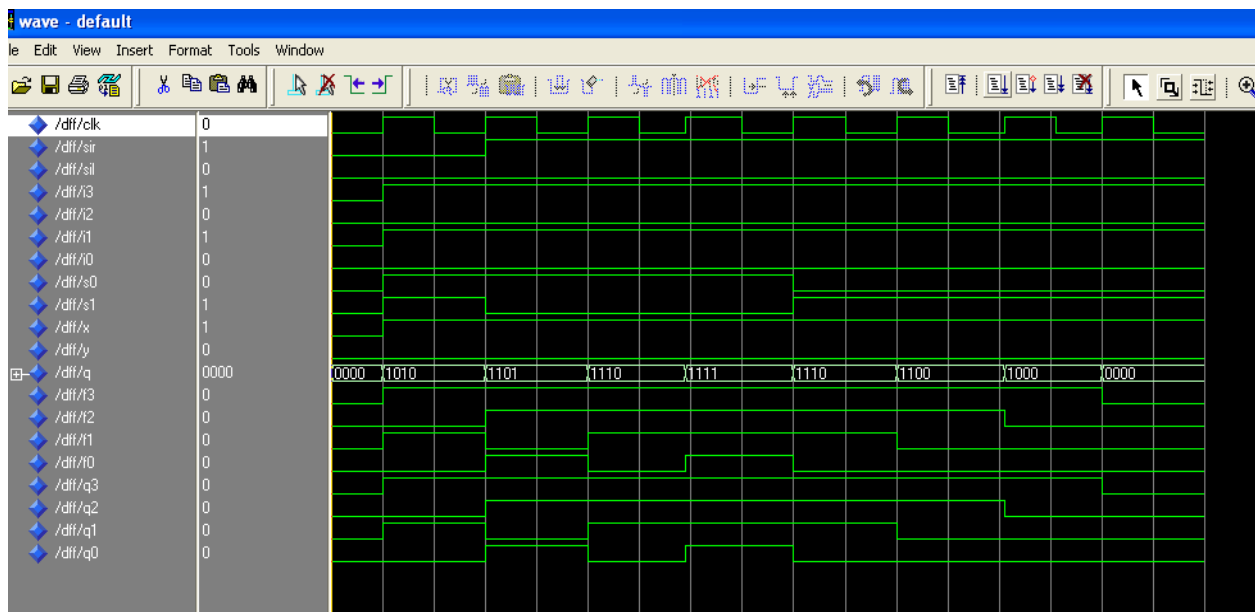


Figure 6. Universal Reversible shift register output waveform.

7. CONCLUSION

In this paper a novel design of reversible universal shift register using reversible logics are proposed. A new reversible RR gate that acts as a 4:1 multiplexer is proposed in this paper whose quantum cost is less than that of fredkin gate when used as a multiplexer. The proposed design can also be extended to a n-bit Reversible Universal shift Register. The proposed design was

done using verilog HDL and observed that the quantum cost and the functional verification of the proposed design is done in Xilinx ISE14.1i.

8. FUTURE ENHANCEMENT

The enhancement of this paper can be extended to a n-bit Reversible Universal shift register and power consumption can be reduced. Thus the proposed circuit can be used for designing large reversible sequential circuits.

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