

International Journal of Computer Science and Mobile Computing

A Monthly Journal of Computer Science and Information Technology

ISSN 2320-088X

IJCSMC, Vol. 3, Issue. 3, March 2014, pg.718 – 721

RESEARCH ARTICLE



DESIGN OF FIFTH ORDER CONTINUOUS TIME-DELTA SIGMA ADC USING SIMSIDES

Bedva Tushar¹, Jai Sachith Paul², Latha R³

¹ bedva.amrabhai@cse.christuniversity.in

² jai.paul@cse.christuniversity.in

³ latha.r@christuniversity.in

Abstract— This paper brief the use of very high precision Noise shaping sigma delta modulation techniques for high applications that require a signal-to-noise ratio and high resolution. A continuous-time delta-sigma A/D modulator with OSR of 40, signal bandwidth of 1.5625 MHz and clocked at 500MHz is implemented. This achieves 78 dB SNR and 12 bits of resolution.

Keywords: Over Sampling Ratio, Signal to Noise Ratio, Digital to Analogue Converters, Delta-Sigma Modulator.

I. INTRODUCTION

The Σ - Δ ADC architecture had its origins in the early development phases of pulse code modulation (PCM) [1]. Delta modulation was first invented at the ITT Laboratories in France by E. M. Deloraine, S. Van Mierlo, and B. Derjavitch in 1946[2,3]. The driving force behind delta modulation and differential PCM was to achieve higher transmission efficiency by transmitting the changes (delta) in value between consecutive samples rather than the actual samples themselves.

The name Sigma-Delta modulator [5] comes from putting the integrator (sigma) in front of the delta modulator. Sometimes, the S-D modulator is referred to as an interpolative coder [4]. The quantization noise characteristic (noise performance) of such a coder is frequency dependent in contrast to delta modulation. As will be discussed further, this noise-shaping property is well suited to signal processing applications such as digital audio and communication. Like delta modulators, the S-D modulators use simple coarse quantizers (comparators). However, unlike delta modulators, these systems encode the integral of the signal itself and thus their performance is insensitive to the rate of change of the signal.

Here in this paper we would like to discuss about architecture of fifth order CT-Delta Sigma ADCs.

II. SIMSIDES SOFTWARE

SIMSIDES (Simulink-based Sigma Delta Simulator) is a time-domain behavioural simulator For SDMs that has been developed as a toolbox in the MATLAB/SIMULINK. SIMSIDES can be used for simulating any SDMs architecture,

implemented with both DT and CT circuit techniques. To this end, a complete list of SDMs building blocks (integrators, quantizers, DACs, etc) is included in the toolbox.

The behavioural models of these building blocks take into account the most critical error mechanisms of different circuit techniques including SC, SI, and CT circuits. This technique drastically increases the computational efficiency in terms of CPU time and accuracy of the simulation results.

The behavioural models included in SIMSIDES have been compiled and tested in a number of operating systems, including Apple OS X, UNIX (Solaris), Linux, and Microsoft Windows. Both 32-bit and 64-bit system platforms have been successfully tested in the majority of them.

Although SIMSIDES was originally developed using MATLAB 6.5 and SIMULINK 5, the toolbox has been updated and successfully used in a number of MATLAB/SIMULINK versions in the last years.

III. ADC ARCHITECTURE

A typical delta-sigma ADC for wireless applications has been used to demonstrate the decimation filter design flow. The CT Delta-sigma modulator [6] was designed to satisfy the specifications of the next-generation wireless applications by incorporating a 5th-order loop-filter and a 1-bit quantizer. Figure 1 shows the block diagram of the modulator employing a 5th-order, feed-forward, continuous time loop-filter.

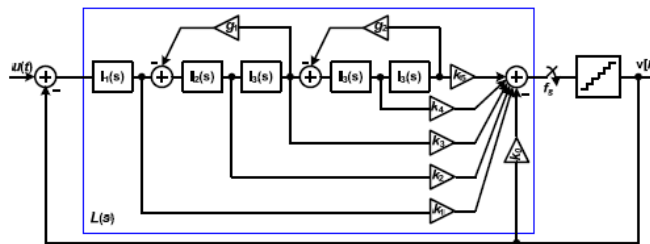


Fig.1 Continuous Time Delta-Sigma Modulator [8]

IV. SIMULATIONS

The block diagram given in the figure 2 shows an Σ - Δ ADC of order 5. The simulation is carried out using Simsides/Simulink [7].

The output of sine wave generator is led to a five level circuit comprising of an integrator and gain to a summer. The output from the summer is led to a single bit quantizer. A digital to analogue convertor is provided in order to convert the digital output from the comparator in to analogue form which is fed back to the integrator.

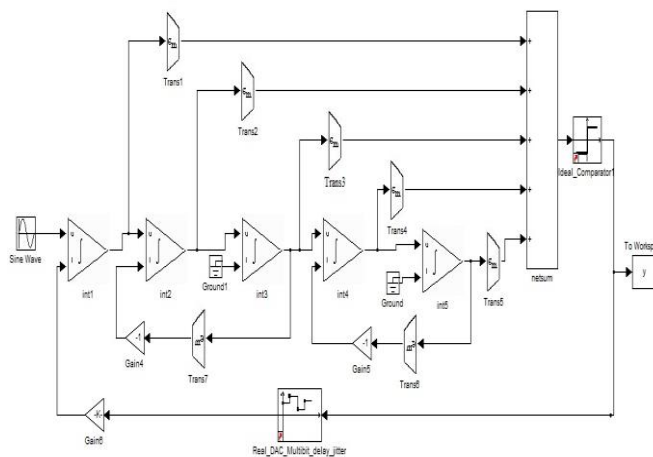


Fig 2. Simulink diagram of 5th order CT Σ - Δ ADC Modulator in Simsides/Simulink[9].

V. RESULTS

The figure 3 shows node spectrum analysis of above Simulink model for signal bandwidth of 1.5625 MHz, OSR=40 and sampling frequency of 500 MHz.

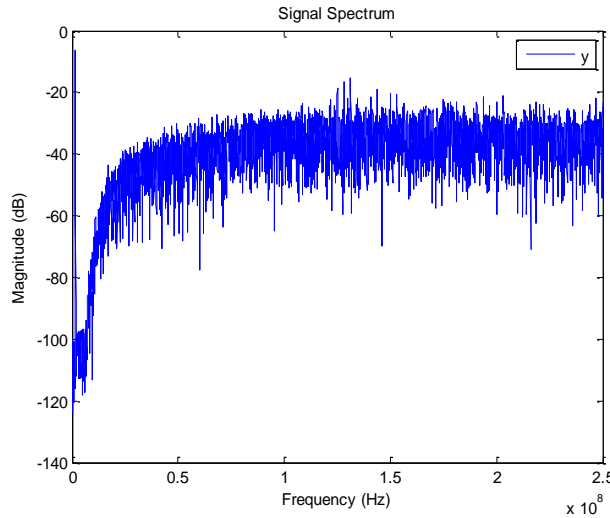
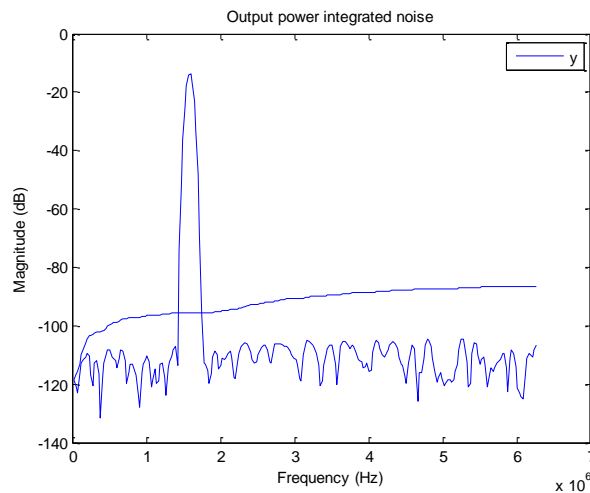


Fig. 3 Node Spectrum Analysis.

Below figure 4 shows integrated power noise with signal spectrum and harmonics in noise power.



From depicted above Simulink architecture calculated SNR is 78.2889 dB (in dB) and 12.7112 bits (in bits) in SIMSIDES/SIMULINK. Here number of bits shows resolution of Delta-Sigma ADC.

VI. CONCLUSION

We presented the design and simulation of a fifth order CT-Delta-Sigma modulator using SIMSIDES/SIMULINK. The measured SNR at 1.5625 MHz signal bandwidth is 78.2889 dB and Effective Number of Bits is 12.7112 bits.

REFERENCES

- [1] K. W. Cattermole, *Principles of Pulse Code Modulation*. London, England: Uliffe, 1969.
- [2] E. M. Deloraine, S. Van Mierlo, and B. Derjavitch, "Methode et système de transmission par impulsions," *French Patent 932,140*, issued August, 1946. Also *British Patent 627,262* issued 1949.

- [3] E. M. Deloraine, S. Van Mierlo, and B. Derjavitch, "Communication System Utilizing Constant Amplitude Pulses of Opposite Polarities," *U.S. Patent 2,629,857*, filed October 8, 1947, issued February 24, 1953.
- [4] W. L. Lee and C. G. Sodini, "A topology for higher order interpolative coders," *Proc. International Symposium on Circuits and Systems*, pp. 459-462, May 1987.
- [5] R. Schreier and G. Temes, *Understanding Delta-Sigma Data Converters*. IEEE press Piscataway, NJ, 2005.
- [6] J. Candy and G. Temes, *Oversampling Delta-Sigma Data Converters (Theory, Design, and Simulation)*, 1991.
- [7] J. Ruiz-Amaya, J. M. de la Rosa, F. Medeiro, F. V. Fernandez, R. del Rio, B. Perez-Verdu, and A. Rodriguez-Vazquez, "MATLAB/SIMULINK based high-level synthesis of discrete-time and continuous-time delta sigma modulators," in *Design, Automation and Test in Europe Conference and Exhibition, 2004*.
- [8] *Efficient Design and Synthesis of Decimation Filters for Wideband Delta-Sigma ADCs*, 2011.
- [9] *MATLAB/SIMULINK-Based High-Level Synthesis of Discrete-Time and Continuous-Time $\Sigma\Delta$ Modulators*, 2004.