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RESEARCH ARTICLE

LOW POWER QVCO USING ADIABATIC LOGIC

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Abstract- A new low-phase noise low-power quadrature voltage-controlled oscillator (QVCO) using adiabatic logic is proposed. Power can be reduced by using this technique. The QVCO is a group of two superposable current-switching distinction Colpitts VCOs in which the major core VCO is affiliated to the second in an in-phase method, and the second core VCO is securely coupled to the first in an anti-phase mode. To syndicate the two core VCOs, the Substrates of the cross-connected transistors as well as the substrates of MOS varactors are used; they need not for any additional fundamentals for coupling, which could decrease the noise and decrease the power dissipation. The power is reduced up to 0.02 nW and the frequency range is reduced up to 1.8 MHz compared to existing system.

Keywords: Current-switching Colpitts-oscillator; multiphase; quadrature oscillator; MOS varactor; low power; adiabatic logic

I. Introduction

Power consumption is an increasing anxiety in VLSI circuits. To encounter the energy necessities new logic circuits have been established otherwise to standard CMOS. The so-called adiabatic families reduce energy consumption due to the use of a pulsed power supply**.** Low power circuit strategy has been a main issue in System on Chip (SoC) and VLSI design areas. As the magnitudes of transistors are disappeared into the deep sub-micron region, the effect of static leakage currents becomes more important. This aspect of power consumption can be measured to some level by novel design, but is primarily handled by progress engineering. Adiabatic logics, which disperse less power than static CMOS logic, have been introduced as a promising new approach in low power circuit design. It is expected that adiabatic logic will be a substitute for static CMOS logic especially for the purpose of low power applications. The quadrature VCO is one of the

significant components in direct-transition of fully-integrated radio-frequency transceiver structure. The approach of QVCO mostly considerations on small voltage, low phase noise and low-power. Several types of VCOs are used to create quadrature signals by transformed coupling methods. One of the most common LC-tank oscillators is the equivalent LC-VCO; this can be coupled to generate quadrature signals using simple coupling ways. This structure has the advantage of generating symmetric waveforms and reducing the up-conversion gain of low frequency noise. The quadrature oscillator is additional kind of phase shift oscillator. In VCO the input signal has some jitter, those jitter will oscillate in normal VCO due to that the delay is increase and it affects the data matching signal. To incredulous this removing jitters by using QVCO. The most representative design for QVCO utilize two differential cross-coupled VCOs with coupling networks to approve the two VCOs work in quadrature phase.

Injection-locked LC quadrature voltage-controlled oscillators (LCQVCOs) conventional on First-harmonics and super-harmonics, injection have become generally popular in RF circuits. Through RF circuit design, low power consumption is a very important consideration; the voltage controlled oscillator (VCO) in a wireless communication also shows an important role. The machinery of current reuse and low voltage supply for low power consumption, such as less than 1mW voltage controlled oscillator (Sub-1mW VCOs). LC-QVCOs have two main parts: a pair of identical LC-VCOs and a coupling system, both of which contribute to the overall QVCO performance. Improving the coupling network by using a variability of active or passive components. In the Colpitts QVCOs extra devices are used for coupling; this can let dispirited the overall operation of the QVCO and increase the chip area. Additionally, any divergences among coupling procedures may disturb the balance of the circuit, leading towards phase inaccuracy. This work delivers a new low-phase noise low-power quadrature voltage-controlled oscillator in which two identical current-switching differential Colpitts VCOs are together without excess coupling devices that could possibly degrade the phase noise and power intake. In this paper the Section II enclosed the proposed QVCO using adiabatic logic. And the Section III indicates the simulation results. Finally, Section IV is the conclusion.

II. THE PROPOSED QVCO USING ADIABATIC LOGIC

The adiabatic logic families suggested in the works are matched with respect to energy consumption, area occupation, and frequency range. Since the application and the distribution of many power clock phases requires additional area and power consumption, logic families with more than four phases are not taken into justification. Moreover, due to the increase of energy dissipation caused by the use of diodes, logic families retaining just MOSFETs are chosen. For these reasons, the resulting three families are chosen: the Efficient Charge Recovery Logic (ECRL), the 2N-2N2P and the Positive Feedback Adiabatic Logic (PFAL). The principal benefit of PFAL over ECRL and 2N-2N2P is that the efficient blocks are in parallel with the communication pMOSFETs. Thus the corresponding resistance is reduced when the capacitance needs to be charged, primary to a fall of the energy dissipation at high frequency. Both share the stuff, that they are worked with a four-phase power-clock. PFAL contains of a latch component designed by two cross-coupled inverters to collect the output state when the input signals are ramped down. ECRL, built on the Cascode Voltage Switch Logic (CVSL), uses a cross-linked PMOS pair as latching constituent. The schematic of the proposed QVCO using adiabatic logic circuit is shown in Fig.1. The circuit is generally involves of two identical switching variance Colpitts VCOs which are interrelated in an “in-phase anti-phase” scheme. Fig. 1 shows, no coupling devices are added together, and thus no extra sources of noise and power consumption are announced. The main part of the switching transistors of the first core VCO are joined to the bulks of the MOS varactors of the second core VCO in an “anti-phase” technique, and the bulks of the switching

transistors of the second core VCO are involved in an "in-phase" way to the differences of the MOS varactors of the first core VCO. Consequently in machinery with P-type wafer the PMOSFETs are located in distinct wells, their bulks can be connected to different possibilities. Substituting transistor can be used for adjusting high power devices such as motors, solenoids or lamps, but they can also use in digital electronics and logic gate circuits. While using the switching transistor, a small base current controls a much greater Collector load current. When exhausting transistors to control inductive loads such as spreads and solenoids, a "Flywheel Diode" is used. When huge currents or voltages important to be measured, Darlington Transistors can be used. MOS varactors functioning the role of coupling devices and permit for the injection path for coupling signals, hence falling the necessity for any superfluous AC coupling capacitors and DC biasing resistors. Furthermore, to get down the noise contribution of the core VCOs to the complete phase noise, the noise-wise higher Colpitts arrangement variations the conventional cross-connected LC-VCOs. Transistor with the drain, source, and bulk associated together. If a varactor is operating in the strong reversal fashion, a transistor with laced source and drain can be used as a creative model since the varactor structure is the same as a MOS transistor.

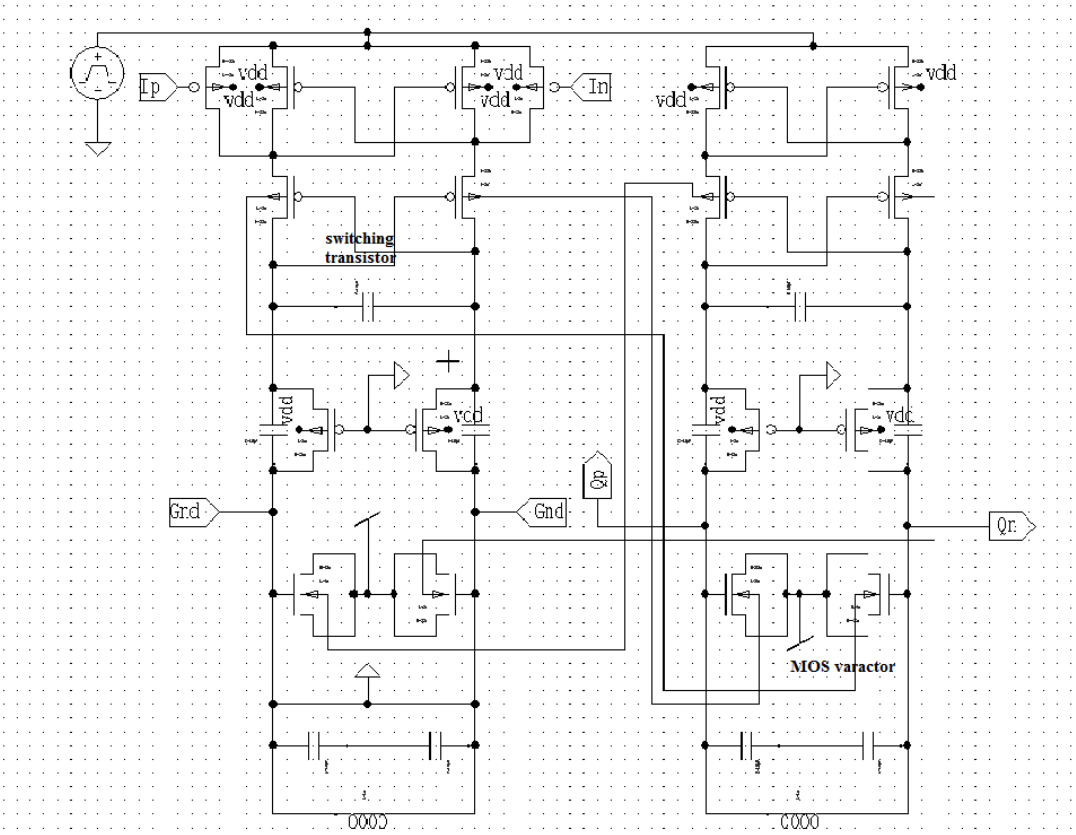

Fig.1 schematic diagram of QVCO using adiabatic logic

III. SIMULATION RESULTS

The predictable quadrature VCO using adiabatic logic is considered and simulated in standard 0.18- m RF-CMOS machinery. According to recreations, oscillation frequency range is 1.8MHz and when Vturn is swept from 0 to 1.8V. Through exhausting Tanner EDA tool the circuit remained simulated Tanner EDA delivers easy-to-use, PC-based electronic design automation (EDA) software solutions for the design,

validation and layout of analog/mixed-signal incorporated circuits, ASICs and MEMS. Its tools systematize and simplify the design progression.

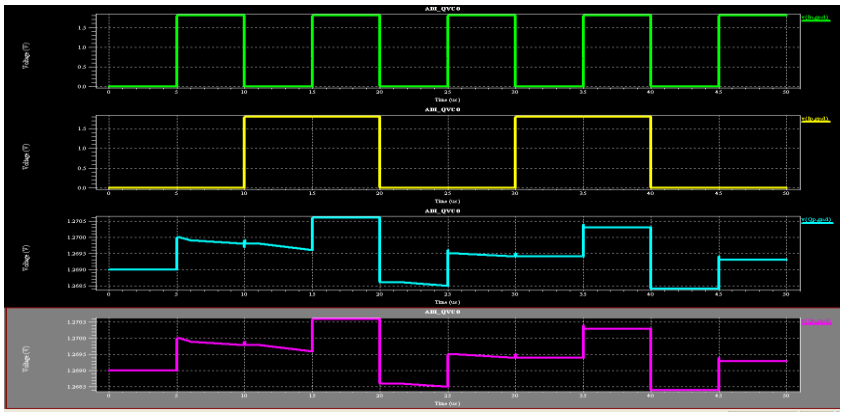

Fig.2 shows output of QVCO using adiabatic logic

Fig.2 labels the organization of QVCO circuit using adiabatic logic with Ip, In inputs and Qn, Qp outputs. Based on the given input the output will be changed if Ip is 1 and In is 1 got proper output.

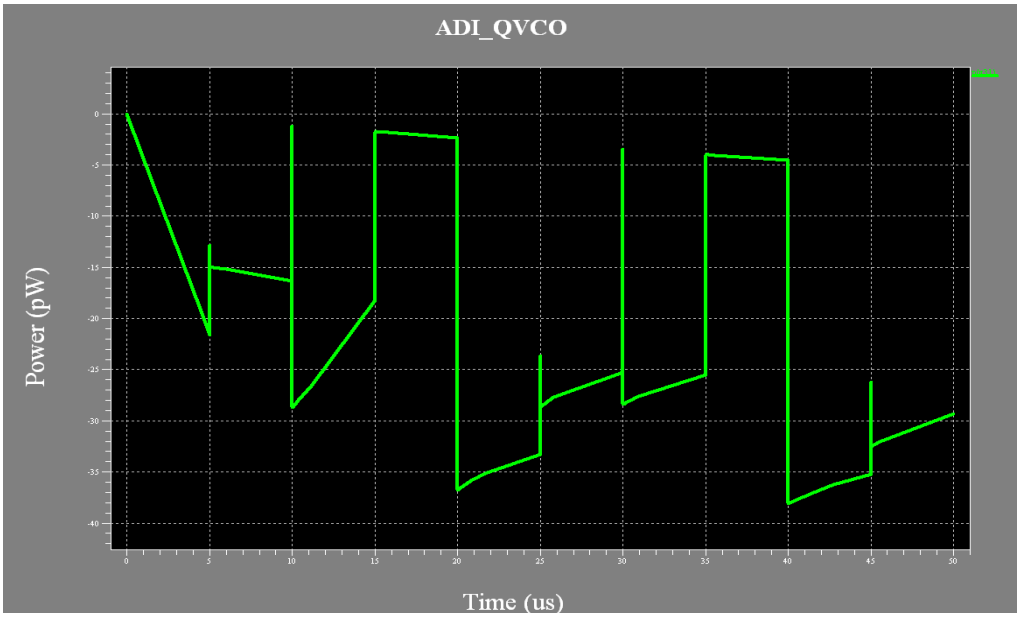

Fig.3 shows the power result of QVCO using adiabatic logic

Fig.3 describes power waveform of Quadrature voltage controlled oscillator circuit using adiabatic logic; the minimum power consumed is up to 0.02nW. The power waveform is obtained power verses time, power in terms of nW and time in terms of µs. Compared to existing system the proposed system power is reduced.

Table 1 Power consumption

Parameters		CMOS technology (μm)	Frequency (Hz)	Power
Existing method	QVCO	0.18	2 MHz	0.18 mW
	Colpitts	0.18	2 MHz	0.016 mW
Proposed method		0.18	1.8 MHz	0.02 nW

IV. CONCLUSION

Injection-locked QVCO using adiabatic logic is typically involves of two different parts: two core VCOs and several coupling devices, in which each portion get to the phase noise performance. Conventional LC-VCOs are replaced with the noise-wise superior current-switching Colpitts VCOs. In accumulation, to lessen the power scattering due to the combinational circuitry, coupling devices were removed by retaining the main part of switching transistors and the bulks of the MOS varactors in the Colpitts important. A consideration of the accomplishment of the proposed QVCO using adiabatic logic of the circuit is available and exhibitions arrangement with simulation conclusions.

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