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RESEARCH ARTICLE

HIGH SPEED AND LOWER HARDWARE COMPLEXITY VLSI ARCHITECTURE FOR LIFTING BASED DISCRETE WAVELET TRANSFORM

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ABSTRACT—A high speed and lower hardware complexity 2-D discrete wavelet transform architecture has been proposed. Previous DWT architectures are based on the modified lifting scheme or the flipping structure. Folded architecture method has been adopted. In the proposed architecture, modifications are made to the lifting scheme, and the intermediate results are combined to form the lifting elements. So as the number of registers can be reduced without extending the critical path., the two-input/two-output parallel scanning architecture is adopted in our design. For a 2-D DWT with the size of N × N, the proposed architecture requires three registers as data memory, and a higher efficiency can be achieved.

Keywords—Discrete Wavelet Transform (DWT), flipping structure, lifting scheme, pipeline, VLSI architecture

I. INTRODUCTION

The Discrete Fourier Transform (DFT) may be thought of in general terms as a matrix multiplication in which the original vector x_k is decomposed into a series of coefficients X_n. Both k and n are integers which range over the same value N.

$$\begin{pmatrix} x_0 \\ . \\ . \\ x_{N-1} \end{pmatrix} = \begin{pmatrix} . & . & . & . \\ . & W_{kn} & . & . \\ . & . & . & . \\ . & . & . & . \end{pmatrix} \begin{pmatrix} X_0 \\ . \\ . \\ X_{N-1} \end{pmatrix}$$

In the above we may derive the transformed coefficients X_n by inverting the matrix. The form of W_{kn} has many possibilities but physically we would like the option of forward and backward transforms i.e., an inverse ought to exist.

The Discrete Wavelet Transform (DWT) generates a matrix W_{kn} which is now widely used for image compression instead of the FT since it is able to localise preserve photographic detail such that many of the coefficients may be ignored (tantamount to filtering) and yet the reconstruction remains effective. For certain types of problems the filtering may be much more aggressive than corresponding FT coefficient filtering. (see "Numerical Recipes in C", Prentice Hall, 2nd Ed. 1992, chapter 13).

DWT's are particularly effective in analysing waveforms which have spikes or pulses buried in noise. The noise may be more effectively removed than with FT filtering and the shape of the pulses preserved. Conservation of Energy similar to a Parseval theorem would also be nice.

II. WAVELETS

A.The Haar Transform to get that Wavelet feel

- Suppose for simplicity we assume an input vector x_k with $0 < k < 7$. This is readily decomposed into an obvious basis set as shown.

$$(x_k) = x_0 \begin{pmatrix}1\\0\\0\\0\\0\\0\\0\\0\end{pmatrix} + x_1 \begin{pmatrix}0\\1\\0\\0\\0\\0\\0\\0\end{pmatrix} + x_2 \begin{pmatrix}0\\0\\1\\0\\0\\0\\0\\0\end{pmatrix} \ldots + x_7 \begin{pmatrix}0\\0\\0\\0\\0\\0\\0\\1\end{pmatrix}$$

- Other basis systems are of course possible (remember your QM and spinors?). In 1910 Haar proposed the following decomposition.

$$(x_k) = a_0 \begin{pmatrix}1\\1\\1\\1\\1\\1\\1\\1\end{pmatrix} + a_1 \begin{pmatrix}1\\1\\1\\1\\-1\\-1\\-1\\-1\end{pmatrix} + a_2 \begin{pmatrix}1\\1\\-1\\-1\\0\\0\\0\\0\end{pmatrix} + a_3 \begin{pmatrix}0\\0\\0\\0\\1\\1\\-1\\-1\end{pmatrix} + a_4 \begin{pmatrix}1\\-1\\0\\0\\0\\0\\0\\0\end{pmatrix} + a_5 \begin{pmatrix}0\\0\\1\\-1\\0\\0\\0\\0\end{pmatrix} + a_6 \begin{pmatrix}0\\0\\0\\0\\1\\-1\\0\\0\end{pmatrix} + a_7 \begin{pmatrix}0\\0\\0\\0\\0\\0\\1\\-1\end{pmatrix}$$

- or $x_n = H_{nk} a_k$ with the columns of H being simply the above basis vectors and the a_k obtained by matrix inversion of H.
- These basis vectors have characteristic "shapes" when drawn on their side as shown in the figure on the next page and it is these shapes which show the essential features of what DWT decomposition does.
- Notice:
  - A mother or scaling function at the start with a non-zero average. This will normally be normalised to 1.
  - Wavelet functions with zero average which are both compressed and translated. It is this compression and translation which finds peaks or pulses well.
  - The wavelet functions are orthogonal. You can see this directly by multiplying any two together.

The wavelet functions have compact support which means they are all localised. This is unlike the FT in which the basis functions $\exp(-2\pi nk / N)$ are continuous.

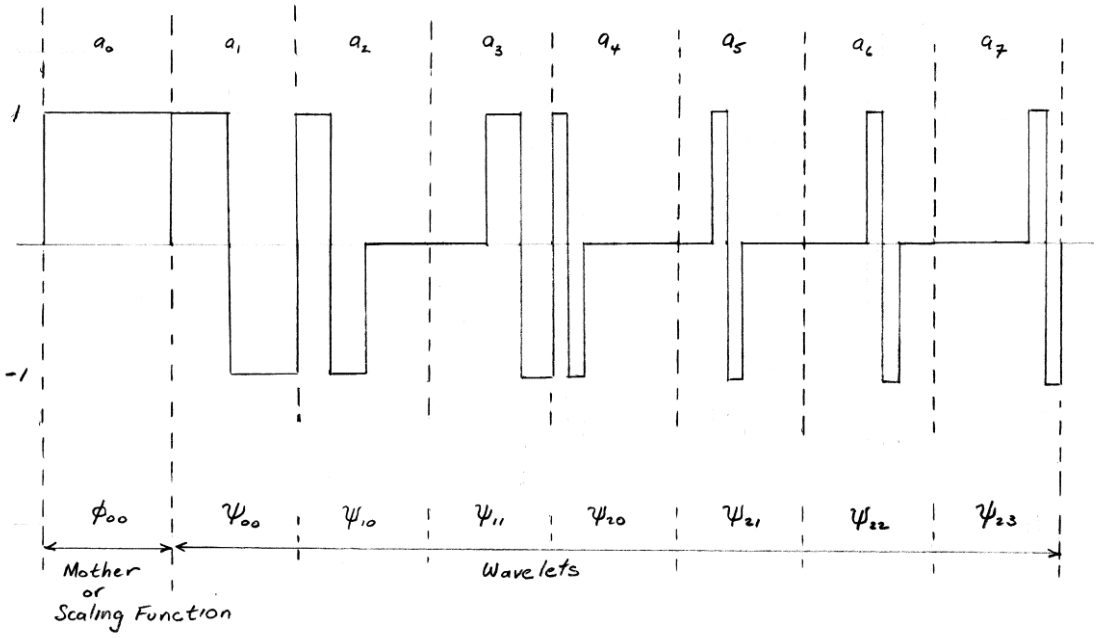


Fig.1.Wavelets

B. Filtering the Coefficients

Filtering of wavelet coefficients is done by removing the smaller coefficients in the difference terms. In these terms are the detail which can often be removed without making a large difference to the overall structure. Two types of filtering exist.

1).*Hard Thresholding:* A difference term is treated as follows: $d = 0$ if $|d| < \lambda$ and otherwise is not touched.

2)Soft Thresholding: As above but all other values for which $d > \lambda$ have the following operation done to them: $d \leftarrow \text{sgn}(d)(|d| - \lambda)$ This repositions the remainder of the coefficients. The literature suggests that λ is best set to $\frac{\sigma\sqrt{2\ln n}}{\sqrt{n}}$. The standard deviation σ is taken over all the difference terms. 'n' is the number of difference terms.

III. LIFTING BASED DWT ARCHITECTURE

Different kinds of lifting-based DWT architectures can be constructed by combining the three basic lifting elements. Most of the applicable DWTs like (9, 7) and (5 ,3) wavelets consist of processing units. This unit is called the processing element (PE). The processing nodes A, B and C are input samples which arrive successively. To implement the predict unit, A and C receive even samples while B receives odd samples. On the other hand, for the update unit, A and C are odd samples and B receives even samples. Now, the structure can be used to implement (5, 3) and (9, 7) wavelets. In this architecture each white circle represents a PE.

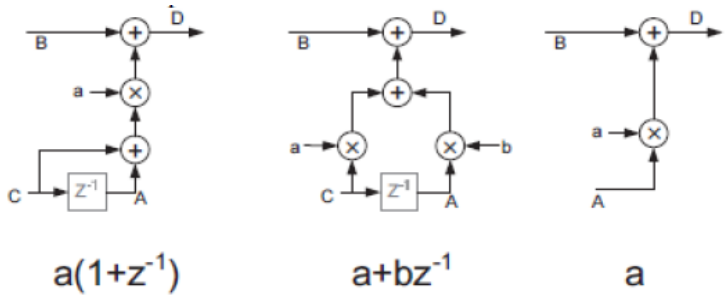


Fig 2 Basic functional units of lifting schemes

The input and output layers are essential (basic) layers and are fixed for each wavelet type, while by changing the number of extended layers, the type of wavelet can be changed accordingly. For example, omission of a single extended (added) layer structure will change the related architecture from (9, 7) type to (5,3) type. The black circles represent needed stored data for computing outputs (s, d). R0, R1 and R2, are registers that get their values from new input samples and are called data memory. The other three black circles which store the results of previous computations are known as temporary memory.

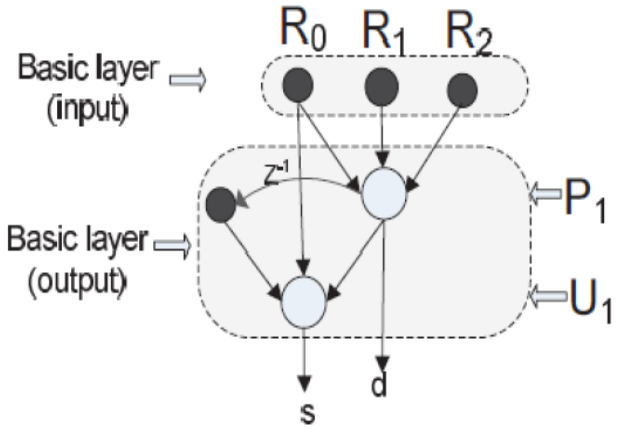


Fig. 3. Lifting structure for (5, 3) wavelet

The number of data memory registers is constant and is equal to 3, whilethe number of temporary memory registers is (2e + 1), where e is the number of extended layers [22]. This structure can be implemented by using combinatorial circuits so that, when the input samples are fed to the architecture, outputs are ready to be used after a delay time. Also, the implementation of the structure can be performed via a pipelined structure by adding some registers. The number of pipeline stages depends on the added registers. Increasing the pipeline stages increases the clock frequency, system latency and number of required registers. So, the sum

of the data and temporary memories in the column-wise DWT unit determines the amount of needed internal memory. The pipeline registers do not affect the required internal memory. The data dependencies in the lifting scheme can be explained with the help of an example of DWT filtering with four factors as in equations [10, 11].The intermediate results generated in the first two stages for the first two lifting steps are subsequently processed to produce the high-pass (HP) outputs in the third stage, followed by the low-pass (LP) outputs in the fourth stage. For (9,7) filter is an example of a filter that requires four lifting steps. For the DWT filters requiring only two factors, such as the (5, 3) filter, the intermediate two stages can simply be bypassed.

IV. MINIMIZING HARDWARE ARCHITECTURES-PARALLEL AND DIRECT MAPPED ARCHITECTURES

A direct mapping of the data dependency diagram into a pipelined architecture was proposed by Liu et al. in [23, 9] .For lifting schemes that require only 2 lifting steps, such as the (5,3) filter consists of two pipeline stages whereas for (9,7) it requires four pipeline stages reducing the hardware utilization to be only 50% or less. The architecture can be sequentially pipelined by combining the previous output of predict stage to current output.

The conventional lifting architectures for (5, 3) and (9, 7) consists of basic processing elements as shown in below Figure The cascaded blocks differ only in multiplier's coefficients. The delay unit represented by z−1 is implemented by one register. Each delay unit contains two consecutive registers. As shown the architecture contains one P and one U unit for (5, 3) wavelet.

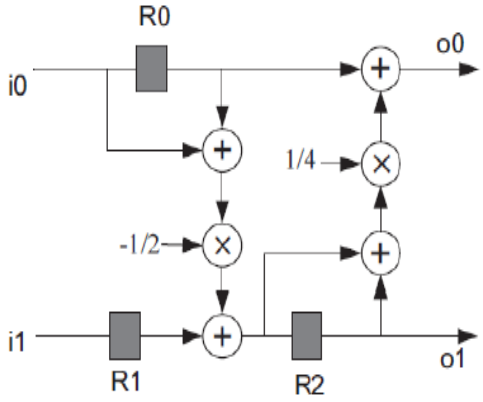


Fig.4. Lifting based hardware architecture for (5, 3) wavelet

From the (5,3) wavelet implementation of the proposed architecture it is clear that only the number of coefficients and delay block registers, that is, the z−blocks, have been modified from four to two. So, changing the wavelet type changes these two quantities, coefficients and registers, only. The architecture for lossy (9, 7) wavelet is shown in Figure 5.

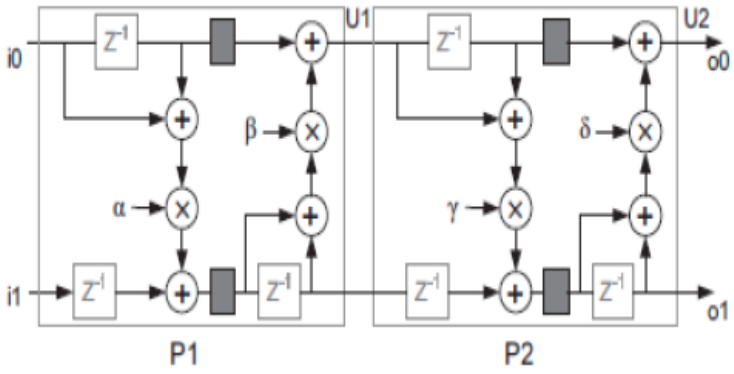


Fig.5. Direct architecture for (9, 7) wavelet

The folded structure is an alternative for the direct mapped architectures as in Figure 5 which the lifting-based structures can be designed systematically. In folded structure, the output of the PE unit is fed back through the delay registers to the PE's input. By adding different numbers of delay registers and coefficients with PE, the structure for different wavelets can be designed.

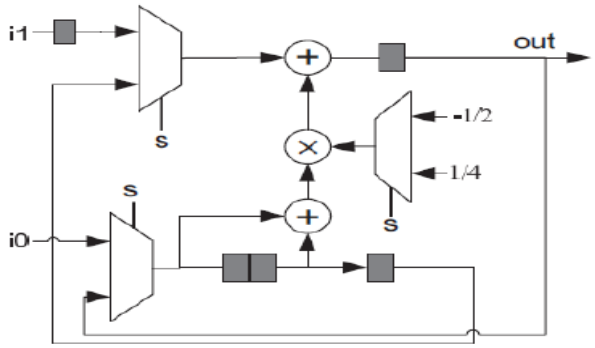


Fig. 6. Folded architecture for (5, 3) wavelet

For example the folded structure for (5, 3) and (9, 7) wavelets have two and four delay registers, respectively. Also the coefficients for (5, 3) wavelet are and while for (9, 7) they are a,b,c,d. The architecture can be reconfigured so that computation of the two phases can be interleaved by selection of appropriate data by the multiplexers.

As a result, two delay registers (D) are needed in each lifting step in order to properly schedule the data in each phase. Based on the phase of interleaved computation, the coefficient for multiplier M1 is either a or c, and similarly the coefficient for multiplier M2 is b or d. The hardware utilization of this architecture is always 100% and the critical path in the multiplier can be reduced.

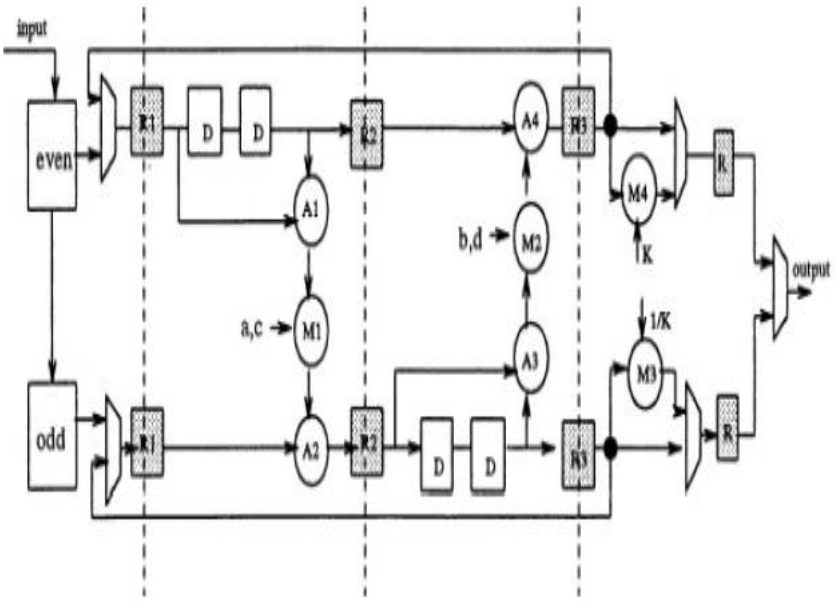


Fig.7. Folded architecture for (9,7) wavelet

V. Flipping Architecture

While conventional lifting-based architectures require fewer arithmetic operations, they sometimes have long critical paths.The critical path of the lifting-based architecture for the (9,7) filter is 4Tm +8Ta while that of the convolution implementation is Tm + 4Ta. One way of improving this is by pipelining which results in a significant increase in the number of registers.For instance, to pipeline the lifting-based (9,7) filter such that the critical path is Tm + 2Ta, 6 additional registers are required. Huang et al. proposed a very efficient way of solving the timing accumulation problem. The basic idea is to remove the multiplications along the critical path by scaling the remaining paths by the inverse of the multiplier coefficients. In the Fig.8.shown the critical path is reduced from 2Tm+3Ta to Tm+3Ta and the reduction rate will increase as the number of serially connected computing units becomes larger.

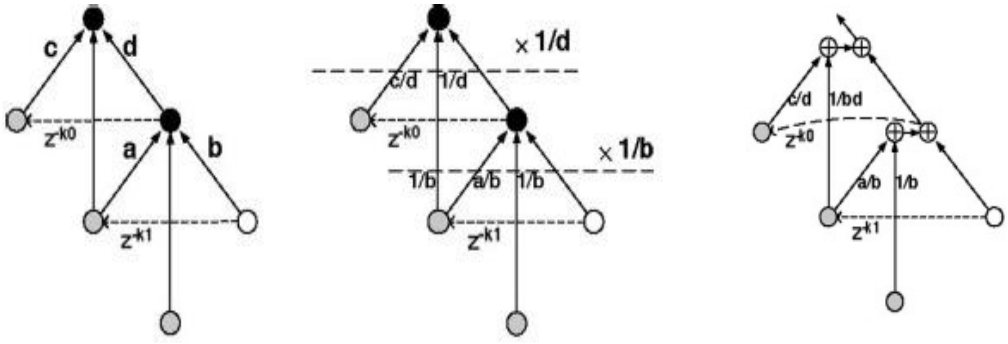


Fig. 8. Flipping architecture (a) Two connected computing units (b) Flipping computing units(c) After splitting the computing units and merging the multipliers.

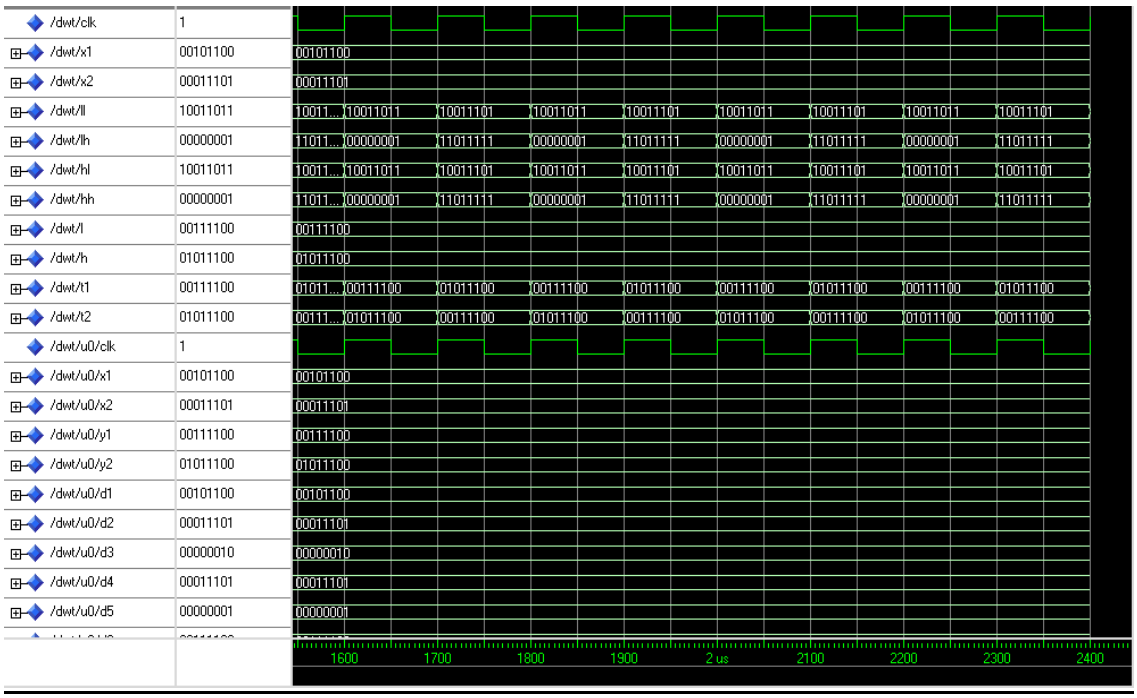
TABLE I

COMPARISION BETWEEN EXISTING ARCHITURE AND PROPOSED

ARCHITCTURE	MINIMUMUM TIME REQUIRED	MINIMUM INPUT TIME BEFORE CLOCK	MAXIMUM O/P TIME REQUIRED AFTER CLK	CRITICAL PATH DELAY	TOTAL EQUIVALENT GATE COUNT FOR DESIGN	ADDITIONAL JTAG GATE COUNT FOR IOBS
Existing architecture	8.712ns	2.245ns	6.347ns	8.49 ns	9,596	2,352
Proposed architecture	5.048ns	2 ns	20.406ns	7.989ns	358	480

VI. Simulation Result

A. 2-D Discrete Wavelet Transform



VII. CONCLUSION

In this , we have proposed a architecture for the 1- and 2-D DWTs.Compared to the previous architectures the folded architecture method has reduced the hardware complexity , no of registers and critical path delay.The proposed method has also reduced the memory space. This review is useful for exploring a new method of pipelined architectures capable of handling multiple data streams suitable for application in image and video processing multimedia real time applications.

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