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RESEARCH ARTICLE

A NOVEL DESIGN OF REVERSIBLE FLOATING POINT ADDER ARCHITECTURE

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Abstract — This project revolves around the design and implementation of floating point adder architecture using reversible logic to improve the design in terms of the number of garbage outputs and the number of gates used. In recent years, reversible logic has emerged as a promising technology having its applications in low power CMOS, quantum computing, nanotechnology and optical computing because of its zero power dissipation under ideal conditions. In this paper, the reversible logic closely follows the IEEE754 specification for binary Floating point adder architecture is done so as to minimize the number of gates used and their garbage outputs. The existing and the proposed floating point adder architectures are designed using Verilog and simulated using Xilinx ISE 9.1 tool.

Keywords— Reversible Gate, Garbage Outputs, Constant inputs, Quantum Cost

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