Available Online at www.ijcsmc.com

International Journal of Computer Science and Mobile Computing

A Monthly Journal of Computer Science and Information Technology

ISSN 2320–088X

IJCSMC, Vol. 3, Issue. 3, March 2014, pg.326 – 331

RESEARCH ARTICLE

Design of Power Gated ML Sensing Low Power CAM

Neelam Sharma S
M. E VLSI Design
Sri Shakthi Institute of Engineering & technology
neelamsharmaece@gmail.com

Abstract
A Content Addressable Memory (CAM) is a memory unit that performs single clock cycle content matching instead of addresses. CAMs are vast used in look-up table functions, network routers and cache controllers. Since basic lookups are performed over all the stored memory information there is high power dissipation. In reality there is always trade-offs between power consumption, area used and the speed. CAMs are popular in network routers for packet forwarding and packet classification, but they are also beneficial in a variety of other applications that require high speed. The main CAM challenge is to reduce power consumption associated with the large amount of parallel active circuitry, without sacrificing speed or memory density. Thus robust, high-speed and low-power ML sense amplifiers are highly sought after in CAM designs. In this work, we introduce a parity bit and effective gated-power technique to reduce the peak and average power consumption and enhance the robustness of the design against process variations.
Index Terms—CMOS, content addressable memory (CAM), match-line

Full Text: http://www.ijcsmc.com/docs/papers/March2014/V3I3201454.pdf