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RESEARCH ARTICLE

FAULT TOLERANT DEFLECTING ROUTER WITH HIGH FAULT COVERAGE FOR ON-CHIP NETWORK

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Abstract*— Continuous scaling of CMOS technology makes it possible to integrate a large number of heterogeneous devices that need to communicate efficiently on a single chip. For this efficient routers are needed to takes place communication between these devices. As the chip scales, the probability of both permanent and transient faults is also increasing, making Fault Tolerance (FT) a key concern in scaling chips. This project, proposes a fault-tolerant solution for a bufferless network-on-chip, including an on-line fault-diagnosis mechanism to detect both transient and permanent faults, a hybrid automatic repeat request, and forward error correction link-level error control scheme to handle transient faults and a reinforcement-learning-based fault-tolerant deflection routing (FTDR) algorithm to tolerate permanent faults.

***Keywords*— Deflection routing; Fault-tolerance; On-line fault diagnosis; Permanent fault; Transient fault**

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