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RESEARCH ARTICLE

HIGH SPEED AND LOWER HARDWARE COMPLEXITY VLSI ARCHITECTURE FOR LIFTING BASED DISCRETE WAVELET TRANSFORM

K.Kokulavani[1], M.Mohankumar[2]

[1]PG Scholar, Department of Electronics & communication Engineering, Sri Eshwar college of Engineering, India

[2]Assistant Professor, Department of Electronics & communication Engineering, Sri Eshwar college of Engineering, India

[1] charmingkoki@gmail.com; [2] mail2mohanphd@gmail.com

ABSTRACT—A high speed and lower hardware complexity 2-D discrete wavelet transform architecture has been proposed. Previous DWT architectures are based on the modified lifting scheme or the flipping structure. Folded architecture method has been adopted. In the proposed architecture, modifications are made to the lifting scheme, and the intermediate results are combined to form the lifting elements. So as the number of registers can be reduced without extending the critical path., the two-input/two-output parallel scanning architecture is adopted in our design. For a 2-D DWT with the size of N × N, the proposed architecture requires three registers as data memory, and a higher efficiency can be achieved.

Keywords—Discrete Wavelet Transform (DWT), flipping structure, lifting scheme, pipeline, VLSI architecture

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