Available Online at www.ijcsmc.com

International Journal of Computer Science and Mobile Computing

A Monthly Journal of Computer Science and Information Technology

ISSN 2320–088X

IJCSMC, Vol. 3, Issue. 3, March 2014, pg.999 – 1003

RESEARCH ARTICLE

Design of Power Optimization using C2H Hardware Accelerator and NIOS II Processor

Mr. Sufiyan B. Mukadam[1], Prof. Abhijit S. Titarmare[2]

[1]PG Student, Communication Engineering, G.H. Raisoni College of Engineering, Nagpur, INDIA
[2]Assistant Professor, Dept. of E&TC, G.H. Raisoni College of Engineering, Nagpur, INDIA
[1] Sufiyan8118@gmail.com; [2] Abhijit.titarmare@raisoni.net

Abstract— The current trend in the silicon industry has been a move steadily towards Chip Multicore Processor (CMP) system to get better outputs. However, chip multicore processors have higher amount of soft errors, which result in degradation of the overall system reliability. Hence, we have been cautious of using CMP architectures for faster-reliable embedded real-time system applications that have high reliability levels. The major use of these processors also states the processor migration tendency. With new technology processor architectures, the older ones are to become vanished sooner. Present the power optimization and detailed reliability analysis of power optimization of single-core and multi-core based systems. The analysis results are then used to compare the power optimization and reliability of CMP architectures with the corresponding reliability of single processor architectures.

To fulfil this requirement, Designs a method for power optimization using NIOS II processor. Reducing power consumption in embedded system that use Field programmable gate array (FPGA) is increasingly important, particularly for battery powered applications or to reduce heat or system cost. You can use parallel algorithms to exploit the parallel architecture of FPGA devices to accomplish more work per clock cycle, allow you to lower the clock frequency per frame. High-level development tools such as System On Chip Peripherals (SOPC) Builder and the NIOS II C-to-Hardware Acceleration Compiler (C2H) has tremendously useful in the power-saving potential of the FPGA hardware by easily adding hardware accelerators and lowering clock frequencies, optimizing power.

Keywords— Chip Multicore Processor; NIOS II Processor; C2H Compiler; FPGA; SOPC

Full Text: http://www.ijcsmc.com/docs/papers/March2014/V3I3201499b12.pdf