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Low Power Wideband Noise Amplifier for 1GHz to 10GHz Wireless Application

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ABSTRACT— A low power wideband noise amplifier (LNA) for 1GHz to 10GHz wireless has presented for wireless application in this dissertation work. Low power wideband noise amplifier is design by using resistive shunt feedback, current reuse, gain flattening techniques, and inductive feedback technique. The high mobility electron transistors are used to improve the Noise Figure (NF) and scattering parameter of the amplifier. Resistive shunt feedback is used to gives the stability of amplifier. The proposed amplifier included input and out matching network. This proposed amplifier gives wideband impedance matching. The current reuse gives doubling the effective transconductance without any extra power consumption or deterioration of output conductance. The current reuse technique gives the best performance for low power and low voltage application. A current reuse scheme is used to lower the power consumption along with inductive series peaking in the feedback path to boost the impedance bandwidth. The Inductive series peaking technique use to enhance the gain, input matching and noise performance. The low noise amplifier is a necessary element in a wideband communication system. The overall performance of low power noise amplifier is analyzed by power consumption, noise figure, S_{11} parameter, and also compared with the other works. The resonance theory and dc analysis are used for designing the elements of amplifier. The LT spice Simulator and spice coding are used to design and simulation of proposed amplifier. The simulation work is carried out by three analysis, AC analysis, noise analysis and transient analysis. The AC analysis is a small signal analysis in the frequency domain. A low power wideband noise amplifier would be preferred in wireless communication GSM, GPS for giving high stability.

KEYWORDS - Current reuse scheme, Wireless communication, Low noise amplifier, Reflection analysis, power dissipation, Inductive feedback technique

I. INTRODUCTION

Wireless sensor networks (WSNs) have become highly sought after in myriad of applications, including health-care, environmental monitoring, industrial settings, and agriculture. The nature of these applications appoints accurate restrictions on the power consumption of a WSN node. As a result, ultra low power (ULP) RF front-end circuits are required to maximize battery lifetime and to allow operation from energy cultivate from the environment.

At the same time, as the feature size in standard CMOS technologies is shrunk, the maximum allowed supply voltage is reduced as well. While operation from a low supply voltage is desirable in systems powered by energy harvesting to minimize conversion losses, it also leads to restriction on the usable circuit topologies and the speed at which they can operate from energy cultivate from environment.

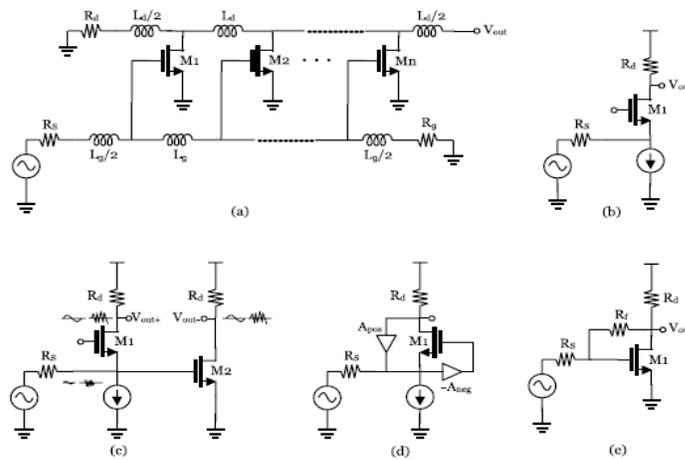


Figure 1: Wideband LNA architectures used in the literature. (a) Distributed amplifier. (b) CG amplifier. (c) Noise cancellation scheme. (d) Using feedback to enhance the performance. (e) Resistive shunt feedback amplifier.

Acceptable the above design challenges and the limitations of CMOS technologies like, higher output conductance, velocity saturation, and mobility debasement, the high transit frequency, f_T , of short channel CMOS technologies can be traded with power consumption to implement low power RF circuits with high bandwidths. This compromise was first highlighted in which a biasing metric is introduced for low-power RF design. This biasing metric does not include the effects of the output conductance, g_{ds} and the drain source voltage V_{DS} on the intrinsic gain, both of which are becoming very important in ultra low voltage (ULV) and ULP designs. To address these issues, this paper suggests an extended biasing metric that is suitable for ULV and ULP low noise designs and demonstrates its applicability by designing an ULP, ULV ultra-wideband low noise amplifier (LNA). The LNA is the first active component in the front-end of the receiver, and is generally considered as one of the most power consumption blocks. The high power consumption stems from the fact that an LNA must provide simultaneous wideband matching, high gain, low noise, and high linearity, all of which typically require high power and high supply voltages. These combined specifications have made the design of low-power and low voltage UWB LNAs a challenging research topic. There are various well-known techniques to design wideband LNAs. A continual approach is to employ distributed amplifiers shown in Figure 1(a), which provide high bandwidths that can span into

the multi gigahertz range. However, distributed amplifiers authorize from high power consumption and occupy a large chip area due to the need for multiple stages and a large number of inductors. Another approach is to use a Common Gate (CG) transistor as the input stage as illustrated in Figure 1(b). A CG transistor provides an impedance of $1/g_m$ at the input, where g_m is the transconductance of the transistor. By setting g_m to 20 mS, a wideband 50Ω input match is achieved. In spite of wideband matching, this strategy faces two major problems. The first is the noise figure (NF) is minimum bounded by $1+\gamma/\alpha$ where γ is thermal noise coefficient and $\alpha = g_m/g_{d0}$ at the matching condition and the second is that the transconductation g_m is bounded by the input matching pattern and cannot be increased to improve the NF and gain, or decreased to reduce the power consumption. Two techniques that have been used to improve CG stage circuit performance are noise cancellation and feedback. A conventional noise cancellation technique in LNAs is demonstrated in Figure 1(c). Noise cancellation techniques have been improving the NF, but this occurs at the cost of higher power consumption due to extra stages and high supply voltages. A combination of feedback and feed forward techniques, shown in Figure 1(d), has been used to break the tradeoffs between NF, gain, and input matching however, the extra stages add parasitic capacitances and limit the bandwidth of operation. These examples show that stretching a low-power and wideband solution with a CG input stage is a challenging task. The resistive shunt feedback design is another applicable solution for wideband LNA design. This involve quarter a feedback resistor around a common source amplifier to realize a wideband 50Ω input match as shown in Figure 1(e) However, there is a trade-off between input matching and the NF of the LNA and satisfying both criteria concurrently generally leads to increased power consumption. As a result, novel circuit design techniques are required to lower the power consumption. This paper reviews the challenges encountered when designing ULP, ULV circuits, and introduces an extended ULP, ULV biasing metric to optimize transistor performance. A combination of circuit techniques that are suitable for ULP, ULV designs are presented, and a broadband resistive-feedback LNA in a 90-nm CMOS technology is designed using these techniques and its measured performance is hanging with state-of-the-art works. The principles in the prospective low voltage and low-power design methodology presented here can be swimmingly adapted and correlated to other RF circuits.

II. LOW POWER WIDEBAND DESIGN CHALLENGES

A. Resistive Shunt Feedback

The resistive shunt feedback architecture is another viable explication for wideband LNA design. This involves placing a feedback resistor around a common source amplifier to realize a wideband 50- input match. The input impedance of this LNA is given by,

$$\frac{r_o \parallel R_L + R_f}{1 + g_m(r_o \parallel R_L)} \quad (1)$$

And its voltage gain can be found by,

$$\frac{(r_o \parallel R_L)(1 - g_m R_f)}{(r_o \parallel R_L + R_f)} \quad (2)$$

The input impedance of the resistive shunt feedback LNA can be controlled through feedback resistor, R_f , and g_m of the transistor. In order to achieve low power input matching, low values of R_f are desired; however, this will lead to low voltage Gain (and high noise figure).

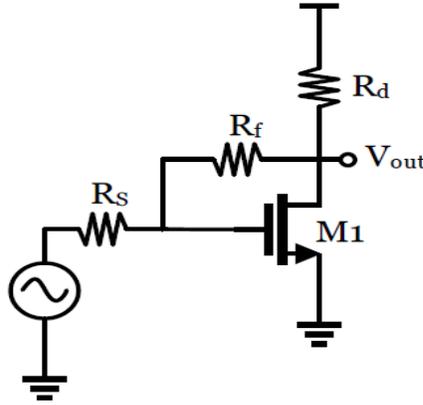


Figure 2 : Schematic Circuit of a resistive shunt feedback LNA, a technique to provide wideband input matching. Hence, this trade-off between input matching and the NF/gain of the LNA, and satisfying both criteria simultaneously generally leads to increased power consumption.

B. Sub-mW Wideband Low Noise Amplifiers

In this section we will review the wideband LNA designs which are consuming less than 1-mW of power. The LNA, as the first active block in the RF front-end of a receiver, has to provide simultaneous wideband matching, low noise, high gain, and modest linearity, all of which require high power consumption.

Ultra-wideband common-gate LNA with a T-match input network and self-body bias is presented. The T-match network which is composed of a series resistance and an inductance is employed to improve the input matching bandwidth at low frequencies.

C. Comparison of Wideband LNAs

Low noise amplifiers in the literature have different gain, bandwidth, noise figure and power consumption. In some designs, the voltage gain, noise figure or the bandwidth is traded with power consumption or supply voltage to implement a low power, low voltage solution. Therefore, a performance figure of merit has to be developed to perform a fair comparison. In this section, we will use a performance figure of merit (FOM) to compare the performance of state-of-the-art LNAs in the literature versus power consumption and supply voltage.

D. Ultra-Low Voltage Design Challenges

The design of power efficient transceivers requires careful optimization at the circuit level. As the feature size in standard CMOS technologies is shrunk, the maximum allowed supply voltage is reduced as well. Supply voltage reduction is desirable in some applications like wireless sensor networks and systems operating on the energy scavenged from the environment to lower the power consumption and the conversion losses in the DC-DC converters.

E. Transconductance Efficiency

The ratio of transconductance to dc drain current (g_m/I_D) is a conventional approach for designing low-power analog CMOS circuits. In this part, the effect of V_{DS} variation on the g_m/I_D will be studied. As V_{DS} gets reduced, the achievable I_D and correspondingly the g_m of the device decrease due to channel length modulation. Interestingly, the I_D and g_m are reduced by the same factor; hence, the g_m/I_D stays almost constant for different V_{DS} values. Figure 1.8

illustrates the simulation results for g_m/I_D curve for two V_{DS} values with respect to the inversion coefficient (IC) for a transistor in the 90-nm CMOS technology with $W = 40 \mu\text{m}$ and $L = 100 \text{ nm}$ using a BSIM4 model.

$$IC = \frac{I_D}{I_{D0}} = \ln^2 \left(1 + e^{\frac{V_{GS} - V_{TH}}{2nU_T}} \right) \quad (3)$$

Where I_{D0} is the technology current as defined by $I_{D0} = 2n\mu_0 C_{OX} U_T^2 (W/L)$. W is the effective channel width, L is effective channel length, n is the substrate factor whose value depends on process and varies from 1 to 2, μ_0 is the carrier mobility, U_T defined as $U_T = kT/q$ is the thermal voltage, C_{OX} is the gate-oxide capacitance per unit area, V_{GS} is the gate–source voltage, and V_{TH} is the threshold voltage.

In general, weak inversion (WI) corresponds to $IC < 0.1$. If $0.1 < IC < 10$ then the transistor is in moderate inversion (MI) and if $IC > 10$ the transistor is in strong inversion (SI). The transconductance efficiency has a maximum in the deep WI region. The efficiency reaches 0.5 of the maximum at the centre of the MI region and decreases in the SI region.

F. Intrinsic Voltage Gain

The intrinsic voltage gain of a MOS transistor is the small signal low frequency gain of a common source MOSFET with an ideal current source as load. This is simply the ratio of g_m/g_{ds} , where g_{ds} is the derivative of I_D with respect to V_{DS} . Drain–source voltage reduction causes the g_{ds} to increase drastically. This variation can be explained through the channel length modulation (CLM) effect. According to CLM, the g_{ds} decreases directly by increasing the gate length and excess drain–source voltage above $V_{DS, sat}$.

Considering the fact that, by reducing the V_{DS} , the g_m decreases and the g_{ds} increases simultaneously, hence, the intrinsic voltage gain of the transistor, g_m/g_{ds} , gets lowered noticeably. g_m/g_{ds} is a good tool to characterize the achievable gain of the device. The simulation results for the intrinsic voltage gain of an nMOS transistor in a 90-nm CMOS Technology with $W = 40 \mu\text{m}$ and $L = 100 \text{ nm}$ for different values of V_{DS} .

G. Transit Frequency

The other important characteristic of a MOSFET that should be studied is the transit frequency, f_T . The f_T of a device is the frequency where the gate-to-drain current gain, h_{21} , is unity for a grounded-source device. The V_{DS} reduction also lowers the f_T . This reduction can be explained by the fact that f_T is proportional to the g_m which decreases by V_{DS} reduction. Figure 1.10 illustrates the simulation results for the transit frequency of an nMOS transistor in a 90-nm CMOS technology with $W = 40 \mu\text{m}$ and $L = 100 \text{ nm}$ for two different values of V_{DS} . As demonstrated on the figure, the achieved f_T for a V_{DS} of 0.2 V decreases by 27% compared with f_T for a V_{DS} of 0.6 V. It should be noted that, when the V_{DS} is at 0.2 V, the peak of the f_T happens at lower ICs since the transistor enters the triode region at higher ICs. This f_T reduction deteriorates the performance, namely, the NF and gain of the RF-front-end circuits.

H. Noise Figure

The noise characteristics of a MOSFET are highly important for LNA design. The minimum NF, NF_{min} , of a MOS transistor is the NF at the optimum source resistance. The NF_{min} also varies with respect to V_{DS} . The NF_{min} is inversely proportional to the square root of g_m and hence increases as the V_{DS} decreases. The simulated NF_{min} of an

nMOS in a 90-nm CMOS technology with $W = 40 \mu\text{m}$ and $L = 100 \text{ nm}$ for two values of V_{DS} . It is interesting to note that the IC in which the minimum happens is almost unchanged.

I. Linearity

Low supply voltages also limit the achievable linearity in LNAs. To further investigate the effect of supply voltage on the nonlinear behaviour of a MOSFET as a weakly nonlinear system, the nonlinear drain current (i_{ds}) of a transistor can be expressed in terms of v_{gs} and v_{ds} by a 2-D Taylor series

$$I_{\text{ds}}(v_{\text{gs}}, v_{\text{ds}}) = g_m v_{\text{gs}} + g_{\text{ds}} v_{\text{ds}} + g'_m v_{\text{gs}}^2 + g'_{\text{ds}} v_{\text{ds}}^2 + g''_m v_{\text{gs}}^3 + g''_{\text{ds}} v_{\text{ds}}^3 \quad (4)$$

Where the Taylor coefficients can be derived from:

$$g_m^k = \frac{1}{k!} \frac{\partial^k I_{\text{DS}}}{\partial v_{\text{GS}}^k}; \quad g_{\text{ds}}^k = \frac{1}{k!} \frac{\partial^k I_{\text{DS}}}{\partial v_{\text{DS}}^k} \quad (5)$$

The cross terms have been ignored for simplicity. It has been known that g''_m is the strongest contributor to the third order distortion in the circuits. However, it will be shown that in deep sub micrometer technologies and specifically at low V_{DS} values, g_{ds} will deteriorate the linearity of the circuit as well.

III. SIMULATION RESULTS

In this chapter discuss about the result analysis along with the system configuration on which experiment performed. This work has used to improve three parameter, S_{11} parameter, Noise figure (NF), and power.

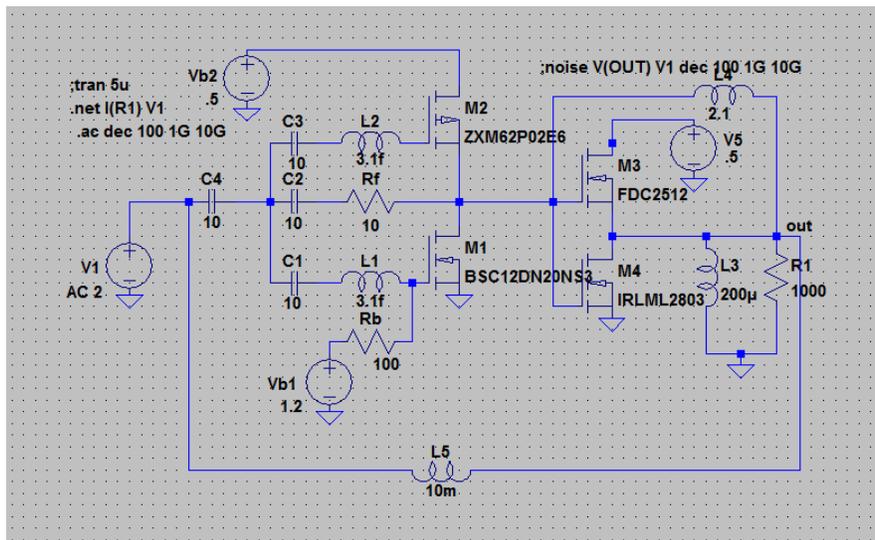


Figure 3: Inductive feedback LT spice design

For simulation use LT spice software. LTspice is freeware computer software establishing a spice simulator of electronic circuits, produced by semiconductor manufacturer linear technology (LTC).It is provide a schematic capture and waveform viewer with enhancements and models to speed the simulation of switching regulators. LTspice IV is macro models for 80% of LTC's switching regulators and operational amplifiers, transistors, MOSFETs, and passive components. It's node-unlimited and third-party models can be imported. Circuit simulations based on transient analysis, AC analysis, noise analysis and DC analysis can be plotted as well as

Fourier analysis. Heat dissipation of components can be calculated and efficiency reports can also be generated. It is used within LTC, and by many users in fields including radio frequency electronics, power electronics, digital electronics, and other disciplines. LTspice IV does not originate printed circuit board (PCB) layouts, but net lists can be imported into layout programs. While it does support simple logic gate simulation, it is not designed specifically for simulating logic circuits. LTspice is also called as Switcher CAD and is sometimes still called by that name. The software is maintained by Mike Engelhard. The application is written for Microsoft windows, it will run under the wind Windows compatibility layer under Linux.

All steps of simulation is:

A. AC Analysis

In this section discuss about reflection parameter (s- parameter). By using AC analysis we can find S₁₁. The AC analysis is a small signal analysis in the frequency domain. In AC analysis, the DC operating point is first calculated to obtain linear, small-signal models for all non-linear components. Then the equivalent circuit is analyzed from a start to a stop frequency. The result of an AC analysis is display in two parts first gain values frequency and second one is phase versus frequency. In AC analysis we can find out quantities, voltage, current, reflection (s-parameter), impedance, admittances with respect to frequency. In this analysis type of sweep is Decade, Number of points per decade is 100, stare frequency 1G, and stop frequency is 10G. By using AC Analysis we find S₁₁.

Click “simulate”, then click “Edit simulation Cmd”.

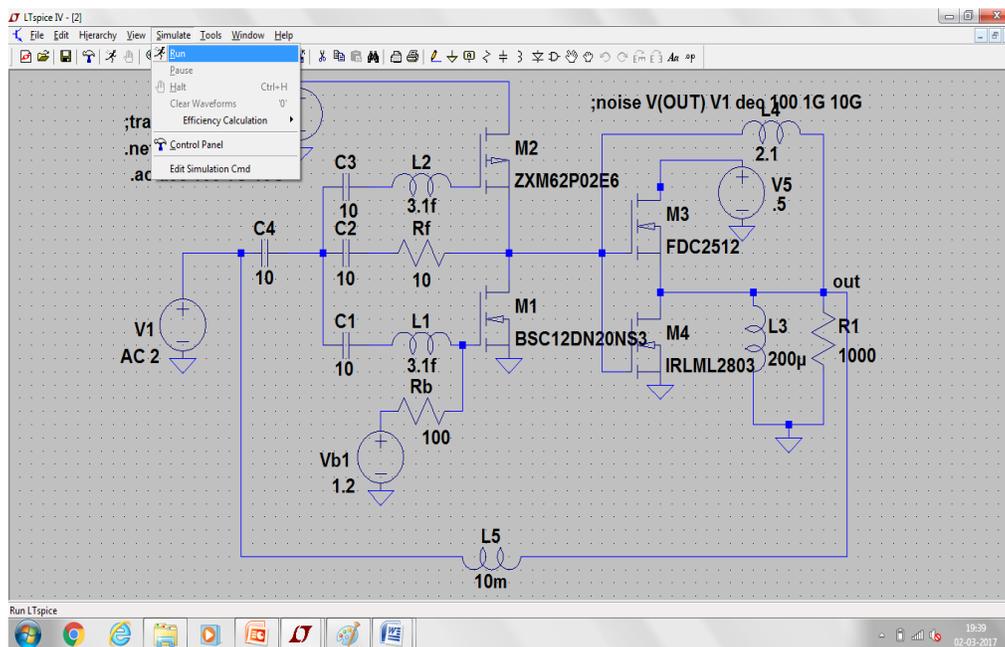


Figure 4 : LT spice AC Analysis simulation

Figure 4 Show LT spice AC simulation step 1. This is LT spice AC analysis open window. This window use to simulate all analysis.

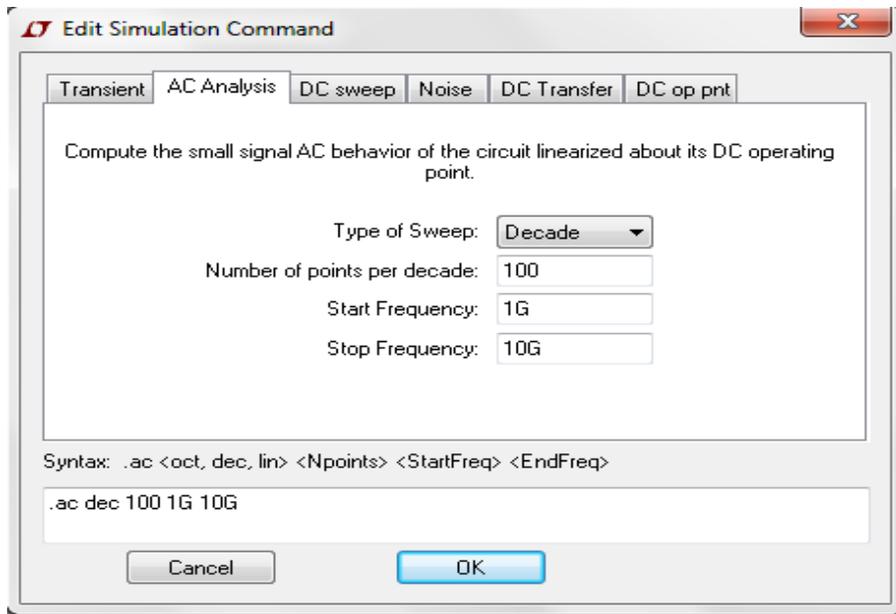


Figure 5 : AC Analysis simulation command

Type of Sweep is “Decade”.

Number of points per decade is “100”.

Start frequency is “1G”.

Stop frequency is “10G”.

.ac dec 100 1G 10G

We can find all parameters in AC Analysis:

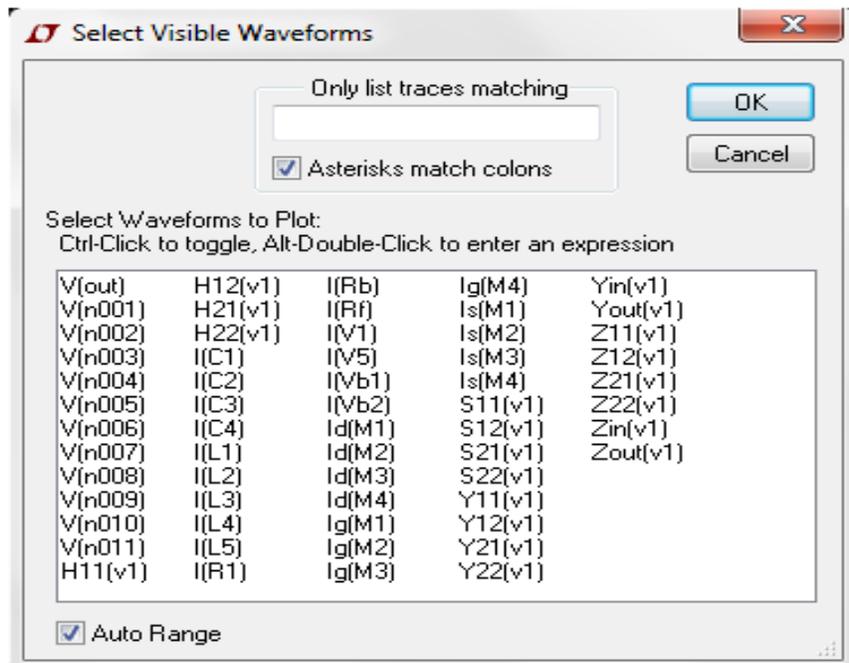


Figure 6: AC Analysis all visible waveforms

Now simulation of S_{11} is:

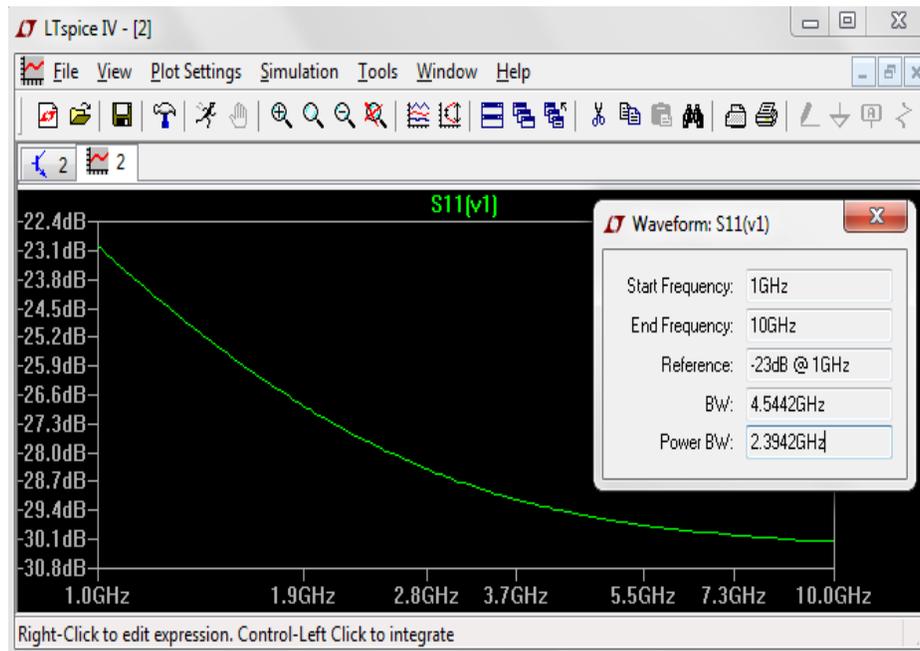


Figure 7: Simulation result S_{11}

Resultant Value of S_{11} is:

Start frequency 1GHz

End Frequency 10GHz

Reference -23dB @ 1GHz

BW 4.5442GHz

Power BW 2.3942GHz

In the theoretical design we calculate the result of S-parameter. In this figure shown that the value of S_{11} parameter under -10dB.

B. Noise Analysis

In theoretical design we calculate the noise figure, output and input. Noise analysis is used to calculate the noise power spectral density generated by a circuit and the total noise power over a specified frequency range. In noise analysis type of sweep is Decade, number of points per decade is 100, starting frequency 1G, and stop frequency is 10G.

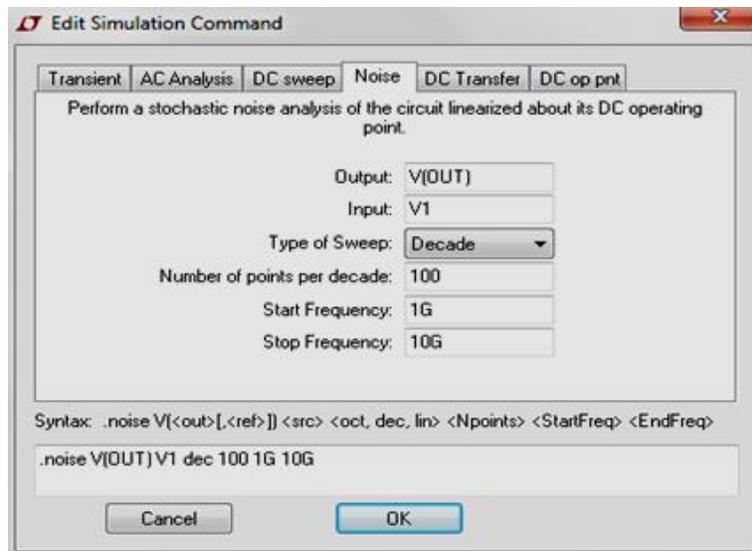


Figure 8: Noise analysis simulation command

In step 2, Output is [V OUT]

Input is [V₁]

Type of sweep (Decade)

Number of points per decade is 100.

Start frequency is 1G.

Stop frequency is 10G.

.noise V [OUT] V1 dec 100 1G 10G

The minimum noise figure (NF), NF_{min} , of a MOS transistor is the NF at the optimum source resistance. The NF_{min} is inversely proportional to the square root of g_m and hence increases as the V_{DS} decreases.

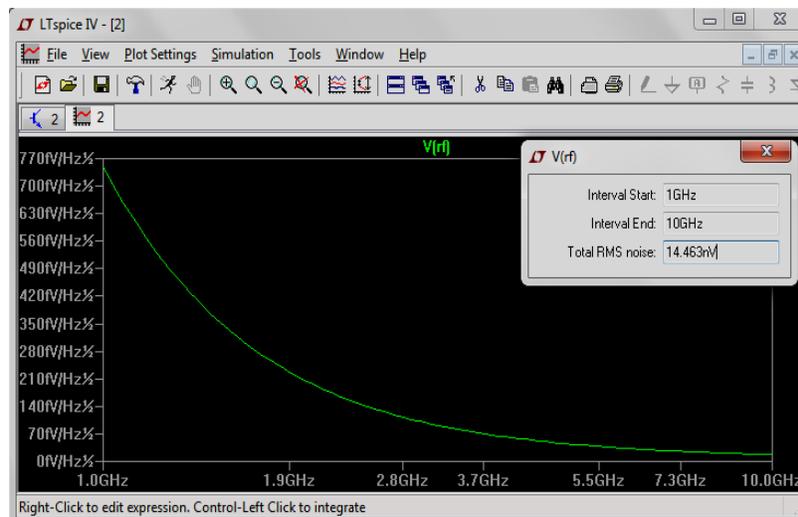


Figure 9: Input Simulation result of noise Analysis

Input result of noise analysis is

Interval start 1GHz

Interval End 10GHz

Total RMS noise 14.463nV

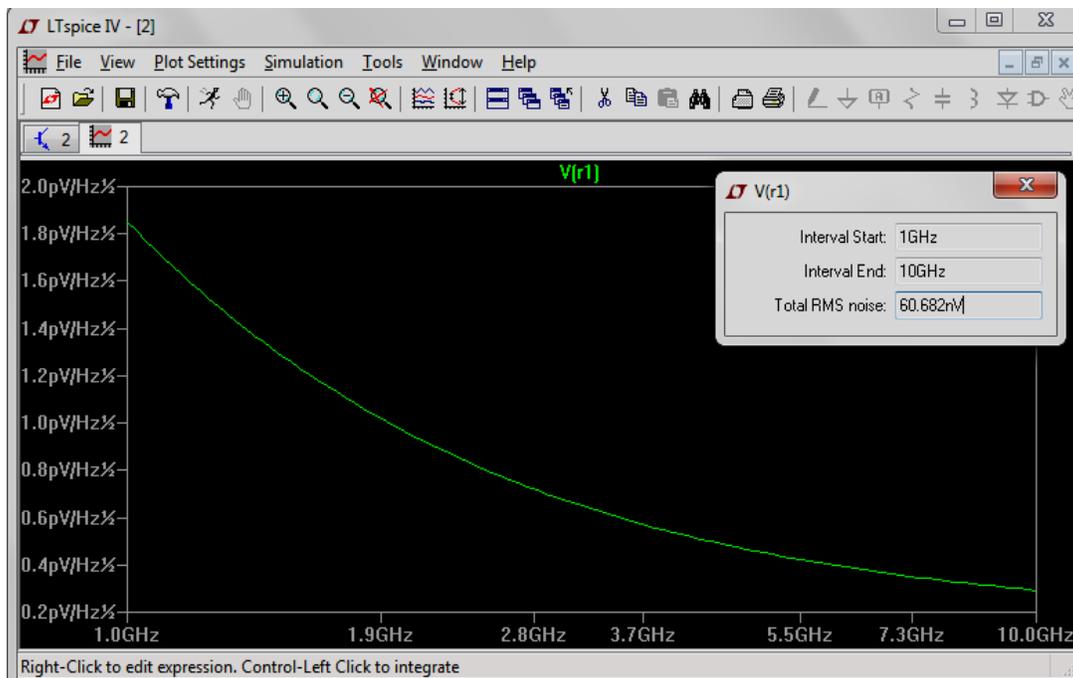


Figure 10: Output Simulation result of noise Analysis

Output result of noise analysis is

Interval start 1GHz

Interval End 10GHz

Total RMS noise 60.682nV

C. Transient analysis

The transient analysis is the calculation of a networks response on arbitrary provocation. The results are network agglomeration branch current and node voltage. Transient analysis is the consideration of energy storing components, i.e. inductors and capacitors. Transient analysis attempts to find an approximation to the analytical solution at discrete time points using numeric integration. In this analysis we take stop time is 5u.

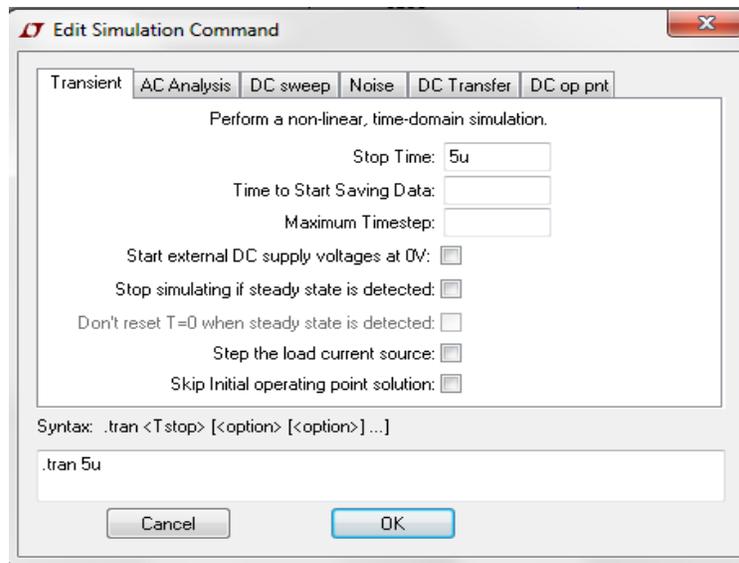


Figure 11: Transient analysis simulation command

In transient analysis stop point is 5u. Then the result of this analysis is,

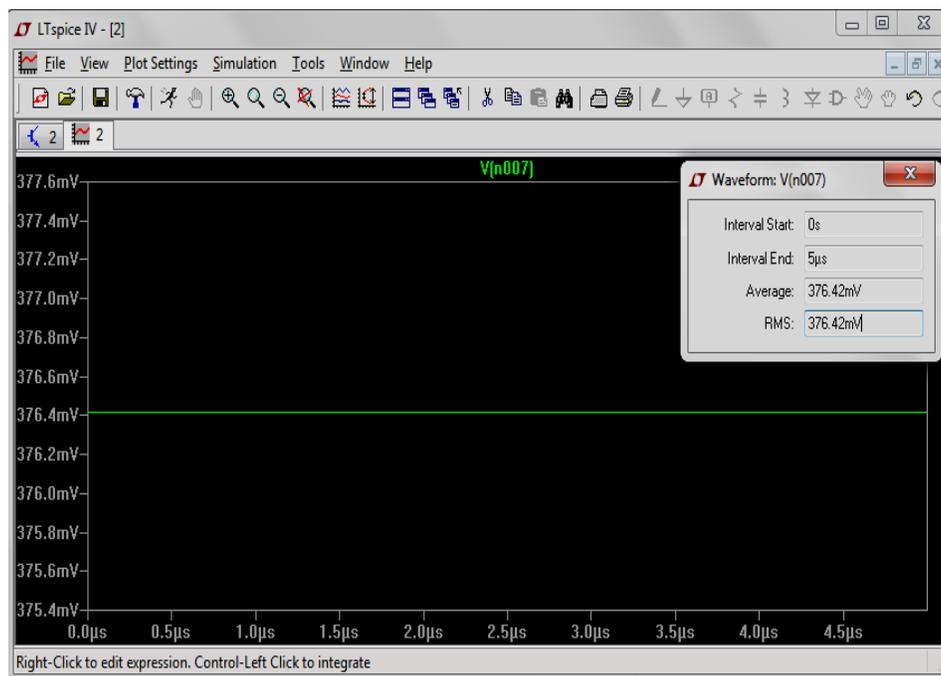


Figure 12: Transient analysis input result

Interval start 0s.

Interval End 5us

Average 376.42mV

RMS 376.42mV

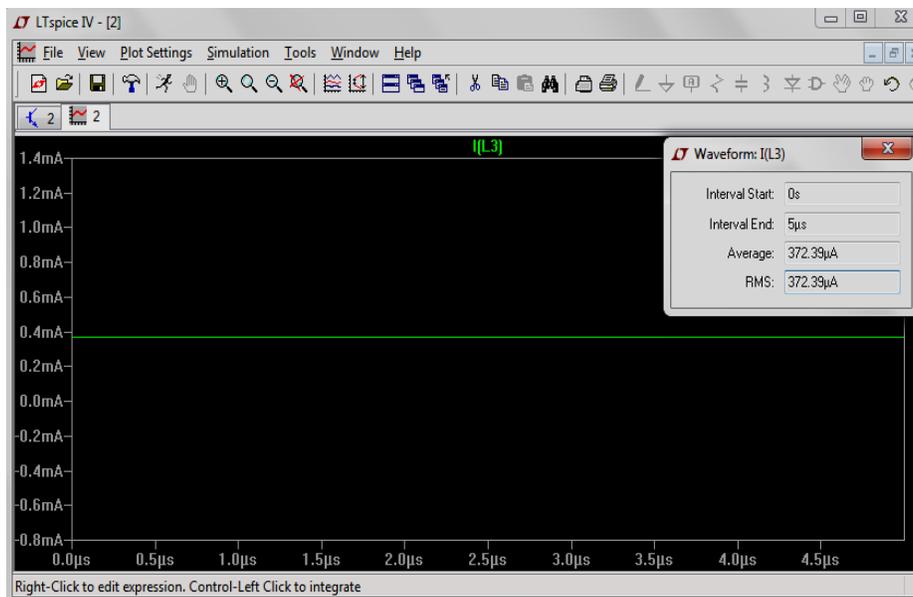


Figure 13: Transient analysis output result

Interval start 0s

Interval End 5µs

Average 372.39µA

RMS 372.39µA.

IV. RESULT AND DISCUSSION

The various designing parameters like Power dissipation, Noise Figure (NF), and S_{11} Parameter are calculated with the help of LT spice simulation software. All the calculated values are shown in table:

TABLE 1 SUMMARIZED SIMULATED RESULTS

S.No.	PARAMETER	SIMULATED VALUE
1	POWER(MW)	0.69
2	SUPPLY(V)	0.5
3	S_{11} (DB)	<-22.7
4	BW	1GHz TO 10GHz
5	NF	UP TO 1

V. CONCLUSION

This dissertation work presented a successfully low power wide band noise amplifier. The design concept is validated through three analyses; AC Analysis, Noise Analysis and Transient Analysis. A low power wide band noise amplifier LNA is proposed and designed based on resistive shunt feedback, current reuse, and gain flattening and inductive feedback technique. A current reuse scheme is used to lower the power consumption, along with inductive series peaking in the feedback path to increase the bandwidth, analyzed and employed in LNA. The overall performance of low power low noise amplifier based on power consumption, noise figure, S_{11} parameter, and also compared with the other works. For better performance of noise figure, S_{11} –parameter and power dissipation the following methodology is used; AC analysis, transient analysis and noise analysis. AC analysis used to find the value of S_{11} parameter. Secondly, noise analysis is employed to find the value of noise figure, and at last, transient analysis is applied to find the value of power dissipation. Resonance theory is employed for improving the performance of the system to reduce the noise figure through an induced feedback inductor and high mobility NMOS transistor. The S parameters is obtained in the range of $S_{11} < -22.4\text{dB}$ in $S_{11} < -10\text{dB}$, BW 1GHz to 10GHz and achieved input output noise figure up to 1 db.

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