**Available Online at www.ijcsmc.com**

**International Journal of Computer Science and Mobile Computing**

**A Monthly Journal of Computer Science and Information Technology**

**ISSN 2320–088X**

***IJCSMC, Vol. 3, Issue. 5, May 2014, pg.515 – 522***

**RESEARCH ARTICLE**

# DESIGN AND ANALYSIS OF SRAM ARRAY STRUCTURES

**S.Divyapriya[1], Dr. P.Ramamoorthy[2]**

[1]PG Scholar, Department of ECE, SNS College of Technology, Coimbatore-35
Email: div06.thi09@gmail.com
[2]Dean, Department of ECE, SNS College of Technology, Coimbatore-35
Email: covairam33@gmail.com

***ABSTRACT***

***Static Random Access Memory (SRAM) is an indispensable part of most modern VLSI Designs, because of its lower power consumption, high speed and its dominates silicon area in many applications. SRAM plays a significant role in energy consumption due to the high density for evermore increased computing power in many ultra-low power applications. A novel low power 6T SRAM cell with single bitline to enhance the stability. SRAM energy efficiencies can be achieved with a wider SRAM array structure with fewer rows than columns particularly at low supply voltage. In the proposed 6T SRAM cell write operation done by charging or discharging single bit line (BL) ,which results in reduction of dynamic power consumption. Simulation results show a better efficiency for the same SRAM bit density and the same supply voltage.***

***Keywords - 8T SRAM, 6T SRAM, Bit density, Energy efficiency, Total power, energy***

## 1. INTRODUCTION

High Energy efficiency is a paramount design constraint in many ultra-low power applications such as portable electronic devices, wireless sensor nodes and implantable biomedical devices. In these applications, SRAM plays a key role in energy consumption due to the high cell density for computational power improvements. One of the most popular ways

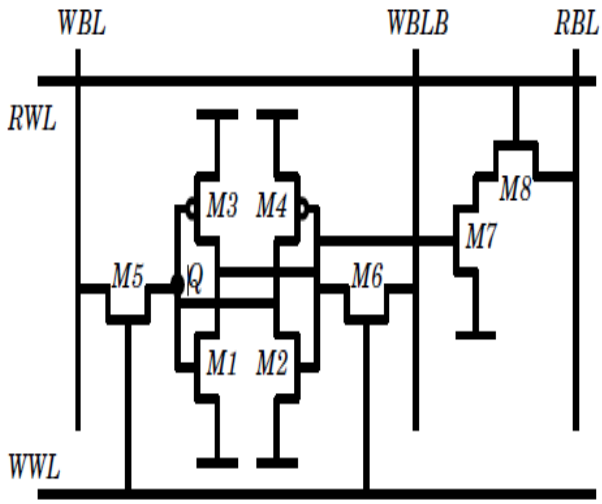
of obtaining minimum energy consumption is to lower supply voltage around or below the device threshold voltage. However, lowering supply voltage generates various design issues. Degradation in cell stability, noise margin, on current to off current ratio and strong sensitivity to process voltage and temperature variations have to be carefully handled for reliable operation. Designing of SRAM in this operation region has been observed to be more challenging due to additional design constraints compared to generic digital logic and so, various circuit techniques have been published with successful hardware measurements. Decoupled SRAM cells have been popularly developed for improving cell stability. Write margin issues have been tackled through several techniques using positively or negatively boosted voltage , strengthening the write access transistors utilizing channel length modulation, and collapsed supply voltage. In addition to supply voltage, SRAM array structure s also influence energy consumption. Evans and Franzon conducted an investigation of the array structures for optimum energy consumption. In their work, the optimum SRAM array structures for minimized energy consumption were found to be non-square and had more rows than columns, while the optimum array structures for minimizing the memory access time were squarer than those for the minimum energy consumption. However, this work only focused on the high performance region where the static energy from the leakage current is insignificant compared to the dynamic energy, which requires the optimal SRAM array structure to be revisited.

Two aspects are important for SRAM cell design: (i) The cell area and (ii) Stability of cell. In today's technology power dissipation in the memory circuits has become an important design consideration. As technology scaling, more devices are integrated into the system, as a result the corresponding leakage power increases .Lower voltages and smaller devices dimensions cause a significant degradation of data stability in SRAM cell, which degrades the output video quality.

## 2. 8T SRAM CELL

The 8T SRAM circuit described in this section. The Schematic of the 8T SRAM cell with transistors sized for a 180nm CMOS Technology shown in figure 1.The primary source of instability problem in SRAM operation is disturbance of bit lines during read operation. The stability in 8T SRAM cell can be enhanced by isolating the read from the write bit lines. The 8T SRAM cell composed of conventional 6T SRAM cell for writing operation and a transistor stack, which can be used for read operation. The Read and write operations are controlled by separate signals Write word line (WWL) and read word line (RWL).




## 3. OPERATION

### 3.1. Read operation

8T SRAM cell has the normal 6T SRAM design with a read decoupled path consisting of two NMOS transistors M5 & M6.Read operation of 8T SRAM is initiated by pre-charging read bit line to full swing voltage. After pre-charging the read bit line ,RWL is asserted that drives access transistor M5 on. If Q=0 then M6 is on &RBL discharges through transistors M5 and M6 to ground. This decreases in the voltage of RBL is sense by the sense amplifier. During read "1" operation, when Q= "1" M6 remains off so there will be no discharge current flow through the read path. In this situation only a very small amount of leakage current flows which is called bit line leakage.

### B. Write operation

In dynamic logic circuits , the two bit lines are recharged initially to power supply (VDD) . When the write enable signal is asserted ,the input data and its complement are placed on the BL and BL bar after that ,asserting "1" on WL one can perform the write operation in the conventional SRAM cell. The bit lines are the most power consuming components in the conventional SRAM cell because of large power dissipation in driving the long bitlines with larger capacitances. Write consumes considerable larger power due to the full voltage swing on the bit lines.

## 4. PROPOSED 6T SINGLE SRAM CELL

The proposed 6T SRAM cell composed of two cross coupled inverters (M0,M1,M4 & M6) and two access transistors (M2 & M3) as shown in Fig 2.Gate terminals of the access transistors are connected to the word lines (WL) .Which is used to select the cell. Source /Drain terminals are connected to the Bit lines

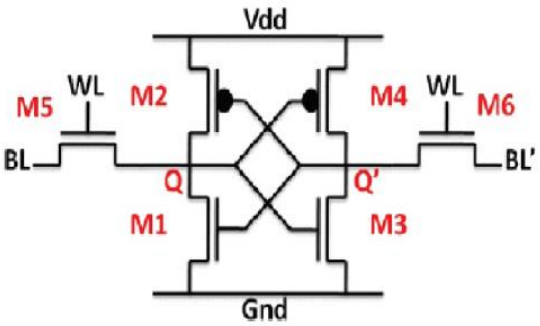



Fig 2. 6 transistor standard SRAM Cell

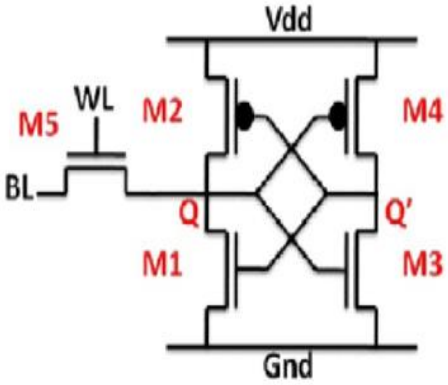



Fig 3.Five Transistor (Single Ended ) SRAM Cell

The proposed design has increased the read stability and SNM , without affecting the size or power consumption of a standard 6 transistor SRAM cell. With the Transistor M6 being taken away a schematic like Fig 3 is obtained, Which still functions like the 6T SRAM but the advantages of this design are reduction in cell area and power consumption. The cell area decreases by one transistor and one bit line .The power consumption from charging the bit line decreases by approximately a factor of 2 because only one bit line is charged during read operation instead of two, and the bit line is charged during a write operation about half of the time (assume equal probability of writing 0 and 1) instead of every time when a write operation is required.

In this array, word lines (WWL and RWL) are shared among cells in one row and bit lines (WBL'S, WBLB'S and RBL'S) are shared among cells in one column.

In order to optimise word and bit lines latency, power and area, SRAM array are broken vertically and horizontally into interleaved sub- arrays. In addition, bit interleaving is used to reduce the probability of upsetting of two bits in one word making using simple and low cost bit correction techniques possible. Accordingly, two adjacent cells in one row belong to two different words.

Hence, an activated row (by WWL or RWL) selects all cells in one row. However, only subsets of cells are intended to be selected. Column selection refers to this issue. The cells that are not intended to be selected are called half selected.

## 5. BITLINE CIRCUITRY

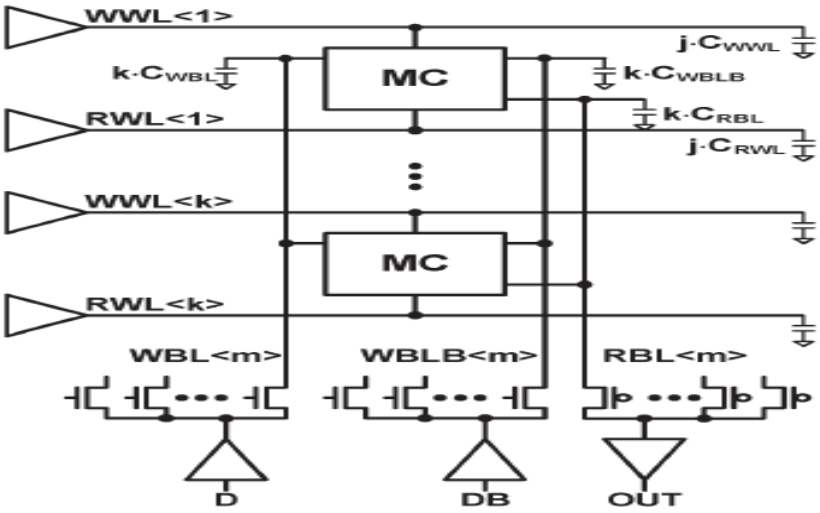



Fig.4 Bit line structure of the SRAM sub array

In figure 2 we show the sequence of steps needed in RMW.

The sequence of steps for RMW is as follows.
1. Precharge circuit charges RBLs.
2. Read word line driver rises RWL to initiate a read operation .In this phase of RMW, multiplexers do not route data to the output.
3. After performing read latches at the bottom of columns store for data.
4. The multiplexer controlled by write back signal loads write drivers.
5. Write is finalized by rising WWL and writing the value on bit lines to the cell.

The number of rows (k) and that of columns(j) can be changed while the products remails constant. In high performance application, they have been mainly selected to meet the system performance requirements. However, in the SRAMs for ultra low power applications, the array structures are limited by design parameter such as cell stability, read bit line sensing margin and leakage current.

## 6. RESULT ANALYSIS

The schematic of proposed 8T SRAM cell was simulated using 180nm CMOS technology to reduce the leakage current and dynamic power consumption. The 8T SRAM cell composed of conventional 6T SRAM cell for writing operation and a transistor stack, which can be used for read operation. The read and write operations are controlled by separate signals write word line (WWL) and read word line (RWL). Fig 5 shows the waveform of 6T SRAM cell.

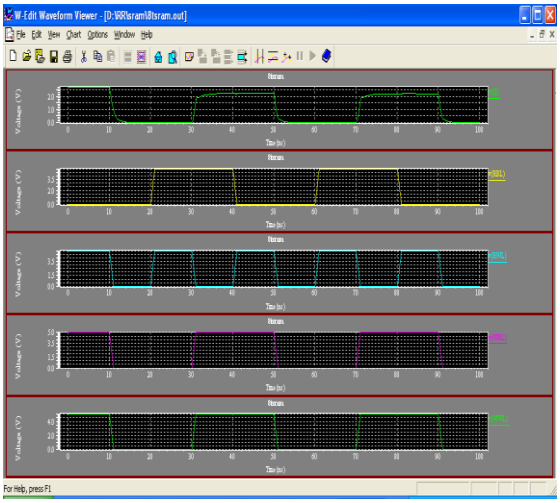


Fig 5 Waveform for 8T SRAM cell

The following fig 6 and fig 7 shows the schematic of proposed 6T SRAM cell and its waveform respectively.

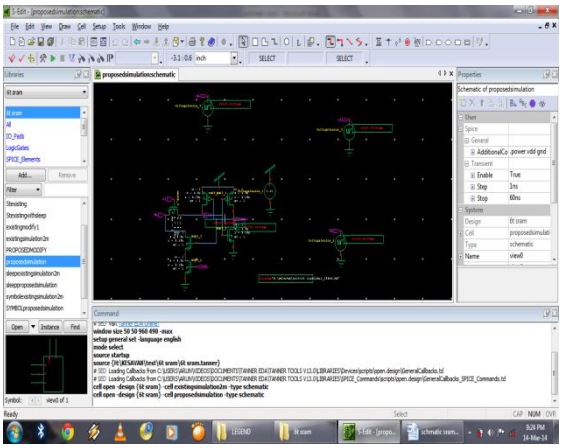


Fig 6 Schematic of proposed 6T SRAM cell

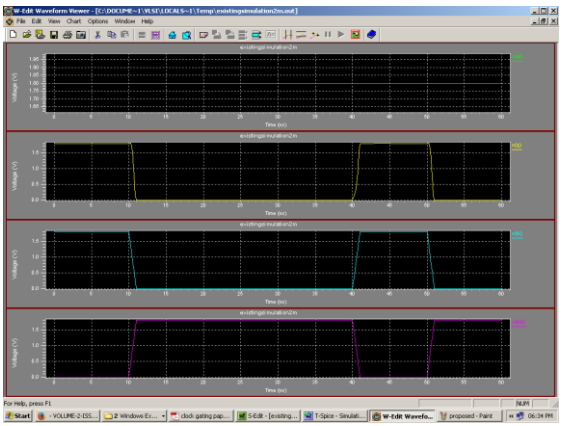


Fig 7 Waveform for proposed 6T SRAM cell

The following table I shows the power results of SRAM structures.

| TECHNIQUES | POWER CONSUMPTION (µW) |
|---|---|
| 8T SRAM | 161.53 |
| 6T SRAM(DUAL BIT) | 24.12 |
| 6T SRAM (SINGLE BIT) | 6.21 |

The following chart shows the comparison of power for various SRAMs

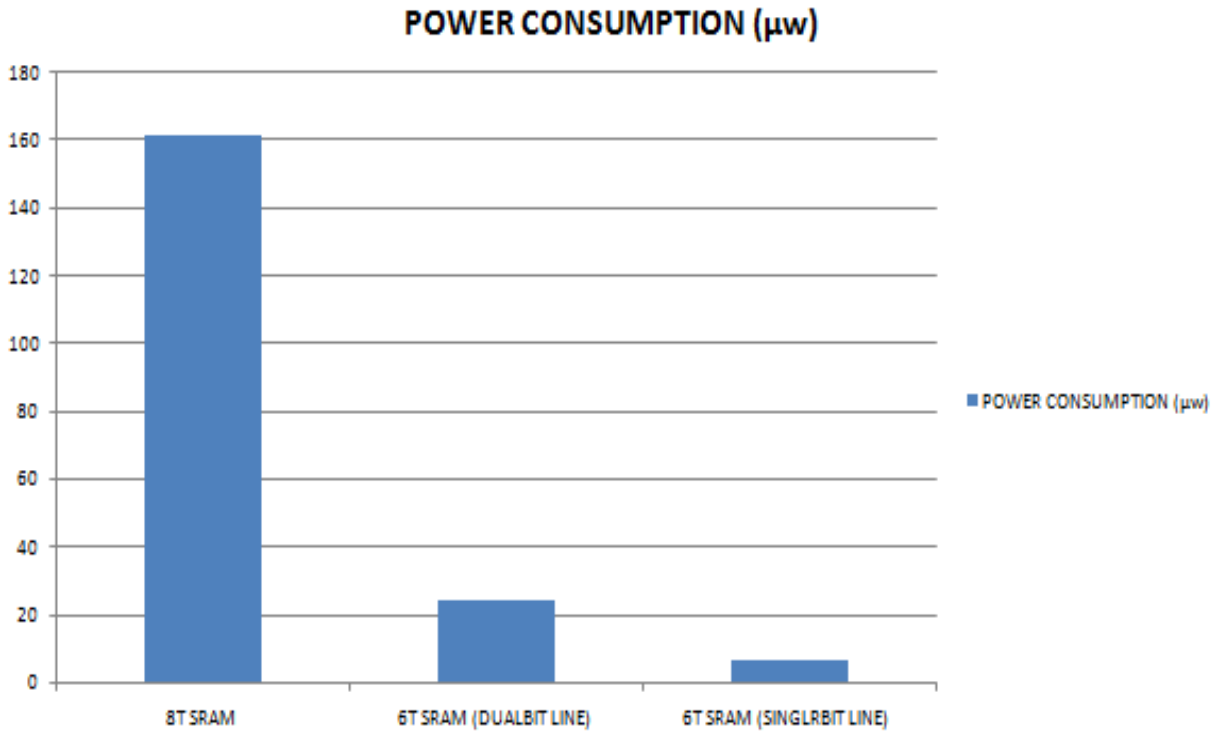



Fig 8 Comparison of power for various SRAMs

## 7. CONCLUSION

Continuing technology scaling puts a limit on how much supply voltage can be scaled. Therefore limiting the power consumption with new architectures are the design requirements in recent integrated circuits. In the case of SRAM, one seemingly counter intuitive approach is to utilize only a single bit line without jeopardizing read stability, which leads to the development of a single ended 6T SRAM. The new SRAM operation scheme, gives a significant power reduction by reducing the amount of switching on bit lines. Extending this operation scheme also allows us to propose a single bit line design that achieves a relatively smaller area while retaining all of the power saving advantages. For a small penalty in delay, singled ended 6T SRAMs are attractive alternatives as memory storage for applications that do not require high clock frequency.

## REFERENCES

[1] V.Subhamkari,G.S.Siva kumar, "Low power single Bit line 6T SRAM cell with High Read stability" International Journal of scientific and Engineering Research, volume 4,Issue 7,July 2013

[2] Yen Chen,Gary Chen et al., "A 0.6V dual rail compiler SRAM design on 45nm CMOS technology with Adaptive SRAM power for lower Vdd_minVLSIs,Solid-State Circuits, IEEE Journal,vol. 44 ,April.2009, Issue 4 , pp.1209-1214

[3] Koichi Takeda et al, "A Read Static Noise Margin Free SRAM cell for Low Vdd and High Speed Applications",Solid-State Circuits, IEEE Journal vol. 41, Jan.2006, Issue 1 , pp.113-121

[4] Jawar Singh, DhirajK.Pradhan et al," A single ended 6T SRAM cell design for ultra low voltage applications",IEICE Electronic Express,2008,pp-750-755

[5] Achiranshu Garg, Student Member, IEEE, and Tony Tae-Hyoung Kim, Member, IEEE,"SRAM array structure for energy efficiency enhancement", IEEE transactions on circuits and systems—ii: express briefs, vol. 60, no. 6, june 2013