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RESEARCH ARTICLE



Analysis of Low Power Flip Flops using an Efficient Embedded Logic

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Abstract- A new dual dynamic node hybrid flip-flop (DDFF) and a novel embedded logic module (DDFF-ELM) based on DDFF are introducing in this paper. The proposed designs eliminate the large capacitance present in the pre-charge node of several state-of-the-art designs by following a split dynamic node structure to separately drive the output pull-up and pull-down transistors. The aim of the DDFF-ELM is to reduce pipeline overhead. It presents an area, power, and speed efficient method to incorporate complex logic functions into the flip-flop. It is implemented using tanner EDA.

Keywords - Flip-flops; high-speed; embedded logic; low-power

I. INTRODUCTION

Technology and speed are always moving forward, from low scale integration to large and VLSI and from megahertz (MHz) to gigahertz (GHz). The system requirements are also rising up with this continuous advancing process of technology and speed of operation. In synchronous systems, high speed has been achieved using advanced pipelining techniques. In modern deep-pipelined architectures, pushing the speed further up demands a lower pipeline overhead. This overhead is the latency associated with the pipeline elements, such as the flip-flops and latches.

Hybrid latch flip-flop (HLFF) and semi dynamic flip-flop (SDFF) are considered as the classic high-performance flip-flops. They possess a hybrid architecture that combines the merits of dynamic and static structures. In addition, SDFF has a distinctive capability of incorporating logic very efficiently, because, only one transistor is driven by the data input. This greatly helps in reducing the pipeline overhead since the delay and area associated with one or more logic stages preceding the flip-flop can be eliminated.

Cross charge control flip-flop (XCFF) has considerable advantages over SDFF and HLFF in both power and speed. It uses a split-dynamic node to reduce the pre-charge capacitance, which is one of the most important reasons for the large power

consumption in most of the conventional designs. But this structure still has some drawbacks, due to redundant power dissipation that results when the data does not switch for more than one clock (CLK) cycles. Also, the large hold-time requirement makes the design of timing-critical systems with XCFF an involved process. Finally, despite having a single data-driven transistor, embedding logic to XCFF is not very efficient due to the susceptibility to charge sharing at the internal dynamic nodes.

In this paper, we propose a new dual dynamic node hybrid flip-flop (DDFF) and a novel embedded logic module (DDFFELM). Both of them eliminate the drawbacks of XCFF. The new designs are free from unwanted transitions resulting when the data input is stable at zero. DDFF-ELM presents a speed, area, and power efficient method to reduce the pipeline overhead. The performance of modern high performance flip-flops are compared with that of DDFF at different data activity. The post layout simulation results in 90 nm UMC process show that the DDFF saves 8% and 10% of the total power dissipated at 50% and 25% data activities, respectively when compared with XCFF. The proposed DDFF-ELM has a maximum power reduction of about 27% compared to its counterparts in SDDFF.

II. FLIP-FLOP ARCHITECTURES

A large number of flip-flops and latches have been published in the past few decades. They can be grouped under the static and dynamic design styles. PowerPC 603 (Fig. 1) is one of the most efficient classic static structures. It has the advantages of having a low-power keeper structure and a low latency direct path. As mentioned earlier, the large D-Q delay resulting from the positive setup time is one of the disadvantages of this design. Also, the large data and CLK node capacitances make the design inferior in performance. Despite all these shortcomings, static designs still remain as the low power solution when the speed is not a primary concern.

The second category of the flip-flop design, the dynamic flip-flops includes the modern high performance flip-flops. There are purely dynamic designs as well as pseudo-dynamic structures. The latter, which has an internal pre-charge structure and a static output, deserves special attention because of their distinctive performance improvements. They are called the semi-dynamic or hybrid structures, because they consist of a dynamic frontend and a static output. HLFF (Fig. 2) and SDDFF (Fig. 3) fall under this category. They benefit from the CLK overlap to perform the latching operation. SDDFF is the fastest classic hybrid structure, but is not efficient as far as power consumption is concerned because of the large CLK load as well as the large pre-charge capacitance. HLFF is not the fastest but has a lower power consumption compared to the SDDFF. The longer stack of nMOS transistors at the output node (Fig. 2) makes it slower than SDDFF and causes large hold-time requirement. This large positive hold time requirement makes the integration of HLFF to complex circuits a difficult process. Also it is inefficient in embedding logic.

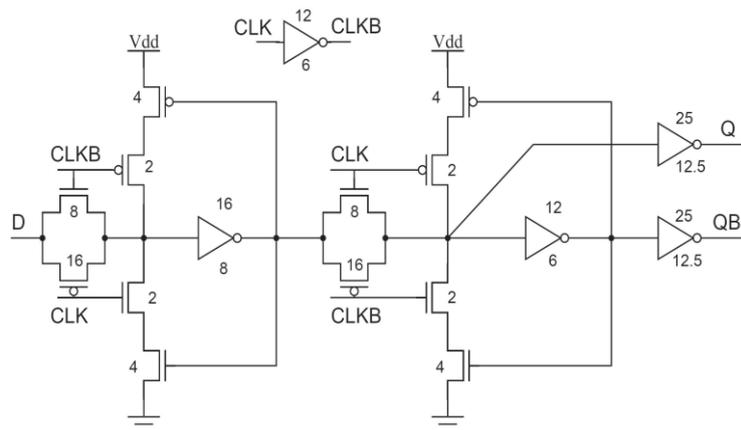


Fig. 1. PowerPC 603 flip-flop

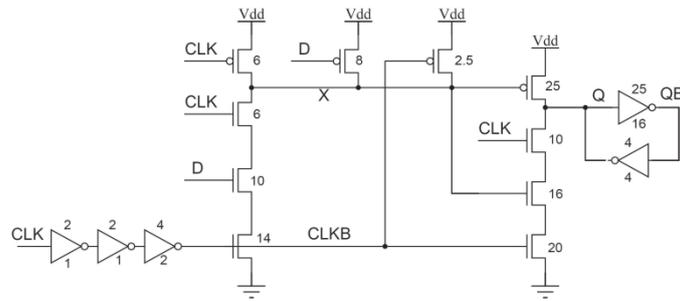


Fig. 2. HLFF

The major sources of power dissipation in the conventional semi-dynamic designs are the redundant data transitions and large pre-charge capacitance. Many attempts have been made to reduce the redundant data transitions in the flip-flops. The conditional data mapping flip-flop (CDMFF) shown in Fig. 4 is one of the most efficient among them. It uses an output feedback structure to conditionally feed the data to the flip-flop. This reduces overall power dissipation by eliminating unwanted transitions when a redundant event is predicted. Since there are no added transistors in the pull-down nMOS stack, the speed performance is not greatly affected. But the presence of three stacked nMOS transistors at the output node, similar to HLFF, and the presence of conditional structures in the critical path increase the hold time requirement and D-Q delay of the flip-flop. Also, the additional transistors added for the conditional circuitry make the flip-flop bulky and cause an increase in power dissipation at higher data activities.

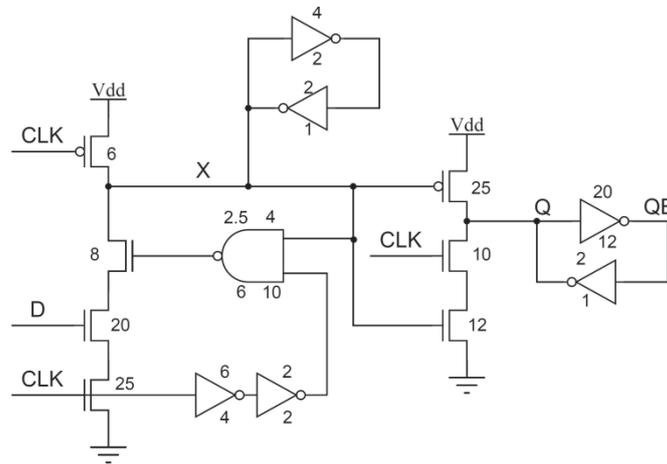


Fig. 3. Semidynamic flip-flop

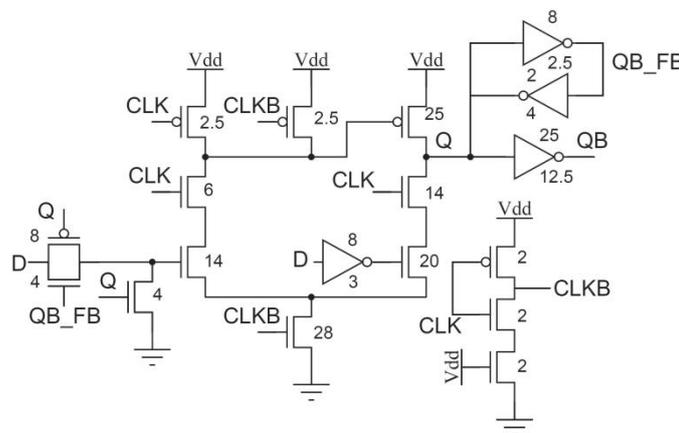


Fig. 4. CDMFF

The large pre-charge capacitance in a wide variety of designs results from the fact that both the output pull-up and the pull-down transistor are driven by this pre-charge node. These transistors being driving large output loads contribute to most of the capacitance at this node. This common drawback of many conventional designs was considered in the design of XCFF (Fig. 5). It reduces the power dissipation by splitting the dynamic node into two, each one separately driving the output pull-up and pull-down transistors as shown in Fig. 5. Since only one of the two dynamic nodes is switched during one CLK cycle, the total power consumption is considerably reduced without any degradation in speed. Also XCFF has a comparatively lower CLK driving load. One of the major drawbacks of this design is the redundant pre-charge at node X2 and X1 for data patterns containing more 0s and 1s, respectively. In addition to the large hold time requirement resulting from the conditional shutoff mechanism, a low to high transition in the CLK when the data is held low can cause charge sharing at node X1. This can trigger erroneous transition at the output unless the inverter pair INV1-2 is carefully skewed. This effect of charge sharing becomes uncontrollably large when complex functions are embedded into the design.

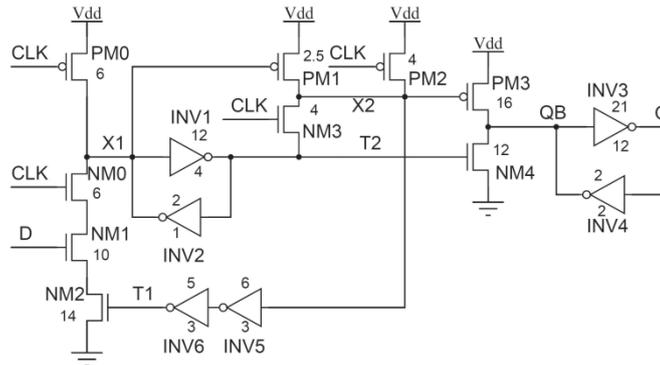


Fig. 5. XCFF

III. PROPOSED DDFF ARCHITECTURE

Fig. 6 shows the proposed DDFF architecture. Node X1 is pseudo-dynamic, with a weak inverter acting as a keeper, whereas, compared to the XCFF, in the new architecture node X2 is purely dynamic. An unconditional shutoff mechanism is provided at the frontend instead of the conditional one in XCFF. The operation of the flip-flop can be divided into two phases: 1) the evaluation phase, when CLK is high, and 2) the pre-charge phase, when CLK is low. The actual latching occurs during the 1–1 overlap of CLK and CLKB during the evaluation phase. If D is high prior to this overlap period, node X1 is discharged through NM0-2. This switches the state of the cross coupled inverter pair INV1-2 causing node X1B to go high and output QB to discharge through NM4. The low level at the node X1 is retained by the inverter pair INV1-2 for the rest of the evaluation phase where no latching occurs. Thus, node X2 is held high throughout the evaluation period by the pMOS transistor PM1. As the CLK falls low, the circuit enters the pre-charge phase and node X1 is pulled high through PM0, switching the state of INV1-2. During this period node X2 is not actively driven by any transistor, it stores the charge dynamically. The outputs at node QB and maintain their voltage levels through INV3-4.

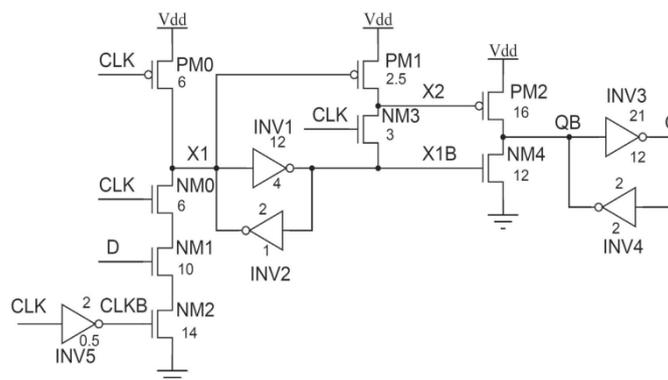


Fig. 6. Proposed DDFF

V. SIMULATION PARAMETERS

It is implemented using Tanner EDA. In which S Edit is for Schematic diagram, T spice is to create a net list and W Edit is the waveform editor.

STEPS FOR SIMULATION RESULTS

- Start-> All programs -> tanner EDA -> S-EDIT
- Click on the symbol browser.
- Select all the components needed for the module to be designed.
- Connect all the components as per the schematic diagram.
- Click on the T-Spice icon.
- The particular technology file to be used is inserted.
- Select “analysis” command from the T-Spice command tool from the dialog box appears.
- Then select “transient analysis” and specify the values, then click “insert”.
- To include the input sources the following procedure is followed:
 - Select the “bit” command from “voltage source” command and enter the specified values, then click “insert”.
 - Select “constant” command from “voltage source” command and enter the bit values of the respective input.
- To include the output waveform to be printed in the W-EDIT screen the following procedure is done.
 - Select “transient results” from the “output” command and enter the specified values and click “insert”.
 - Save and click run icon the top of the screen
 - The input and output waveforms are displayed in the W-Edit window

VI. RESULTS

1. Fig.8 shows the delay comparison of various flip flops. It shows that the proposed DDFF has less delay compared to other flip flops.

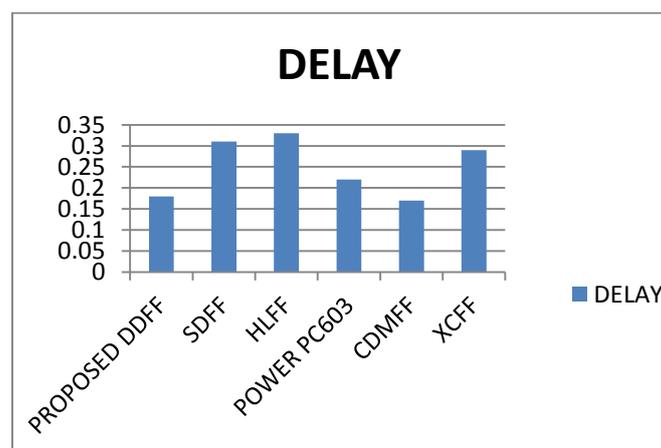


Fig.8 Delay comparison of Flipflops

2. Below table shows the performance comparison of various Flip-Flops

Table 1

PERFORMANCE COMPARISON OF VARIOUS FLIP-FLOPS

	DATA DRIVING POWER (W)	TOTAL POWER (W)	DELAY(ns)	NO. OF TRANSISTOR
Sdff	0.0023	0.17	0.40	27
HLFF	0.0025	0.769	0.28	22
POWER PC 603	0.77	0.0217	0.23	24
CDMFF	0.055	0.280	0.22	24
XCFF	0.005	0.15	0.38	27
DDFF (PROPOSED)	0.002	0.016	0.18	18

3. Below table shows the power and delay comparison of ELM flipflops

TABLE 2

POWER AND DELAY COMPARISON OF ELM FLIPFLOPS

	POWER DISSIPATION (W)	DELAY (s)
Sdff ELM	17.42	0.58
DDFF ELM	6.39	0.67

4. Below Figure shows the comparison between Sdff and Ddff ELM logics.

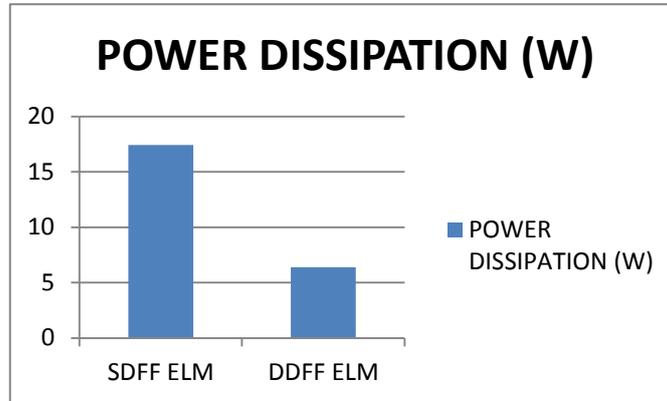


Fig.9 Comparison of power dissipation between Sdff and Ddff ELM logic

VII. CONCLUSION

In this paper, a new low power Ddff and a novel Ddff-ELM were proposed. An analysis of the overlap period required to select proper pulse width was provided in order to make the design process simpler. The proposed Ddff eliminates the redundant power dissipation present in the XCff. By eliminating the charge sharing, the revised structure of the proposed flip-flop, Ddff-ELM, is capable of efficiently incorporating complex logic in to the flip-flop. The presented ELM outperforms the Sdff in the CLK driving power and in internal power dissipation.

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