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RESEARCH ARTICLE

COMPARATIVE STUDY OF LOW POWER PULSE TRIGGERED FLIP-FLOP

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Abstract: Flip-Flops are the critical timing elements in the digital circuits which have large impact on circuit speed and power consumption. The functioning of flip-flop is the important element in determining the efficiency of the system. In this brief a low power flip-flop (FF) based on signal feed through scheme is presented. The proposed design solves the long discharging path problem in conventional explicit type pulse-triggered FF designs and achieves better speed and power performance.
Index terms-Flip-flop, low power, pulse-triggered

I. Introduction

Flip-flops are the basic storage elements used extensively in all kinds of digital designs. Digital designs adopt intensive pipelining techniques and employ many FF-rich modules such as register file, shift register and first in first out. It is also estimated that the power consumption of the clock system, which consists of clock distribution networks and storage elements, is as high as 50% of the total system power. FF's thus contribute a significant portion of the chip area and power consumption to the overall system design. Pulse-triggered FF because of its single latch structure is more popular than the conventional transmission gate (TG) and master-slave based FFs in high speed applications. Besides the speed advantage, its circuit simplicity lowers the power consumption of the clock tree system. A P-FF consists of a pulse generator for strobe signals and a latch for data storage. If the triggering pulses are sufficiently narrow, the latch acts like an edge-triggered FF. Since only one latch, as opposed to two in the conventional master-slave configuration, is needed, a P_FF is simpler in circuit complexity. This leads to a higher toggle rate for high-speed operations. P-FFs also allow time borrowing across clock cycle boundaries and feature a zero or even negative setup time. Despite these advantages pulse generation circuitry requires delicate pulse width control to cope with possible variations in process technology and signal distribution network. To obtain balanced performance among power, delay and area, design space exploration is also widely used technique. In this brief we present a novel low-power P_FF design based on a signal feed-through scheme. Observing the delay discrepancy in latching data "1" and "0" the design manages to shorten the longer delay by feeding the input signal directly to an internal node of the latch design to speed up the data transition. This mechanism is implemented by introducing a simple pass transistor for extra signal driving. When combined with the pulse generation circuitry, it forms a new P-FF design with enhanced speed and power-delay-product performances.

II. Proposed P-FF Design Based On a Signal Feed Through Scheme

PF-FFs, in terms of pulse generation, can be classified as an explicit or an implicit type.IN an implicit type P-FF, the pulse generator is the part of the latch design and no explicit pulse signals are generated. In an explicit type P-FF, the pulse generator and the latch are separate. Without generating pulse signals explicitly, implicit types P-FFs are in general more power-economical. However, they suffer from a longer discharging path, which leads to inferior timing characteristics. Explicit pulse generation, on the contrary, incurs more power consumption but the logic separation from the latch design gives the FF design a unique speed advantage. Its power consumption and the circuit complexity can be effectively reduced if one pulse generator shares a group of FFs. In this brief, we will focus on the explicit type P-FF design.

A. Explicit pulse Data-close-to-output (ep-DCO)

This design contains a NAND-logic-based pulse generator and a semi dynamic true-single-phase-clock (TSPC) structured latch design. In this P-FF design, invertors I3 and I4 are used to latch the data, and the invertors I1 and I2 are used to hold the internal node X. Its circuit diagram is given by the given figure 1.

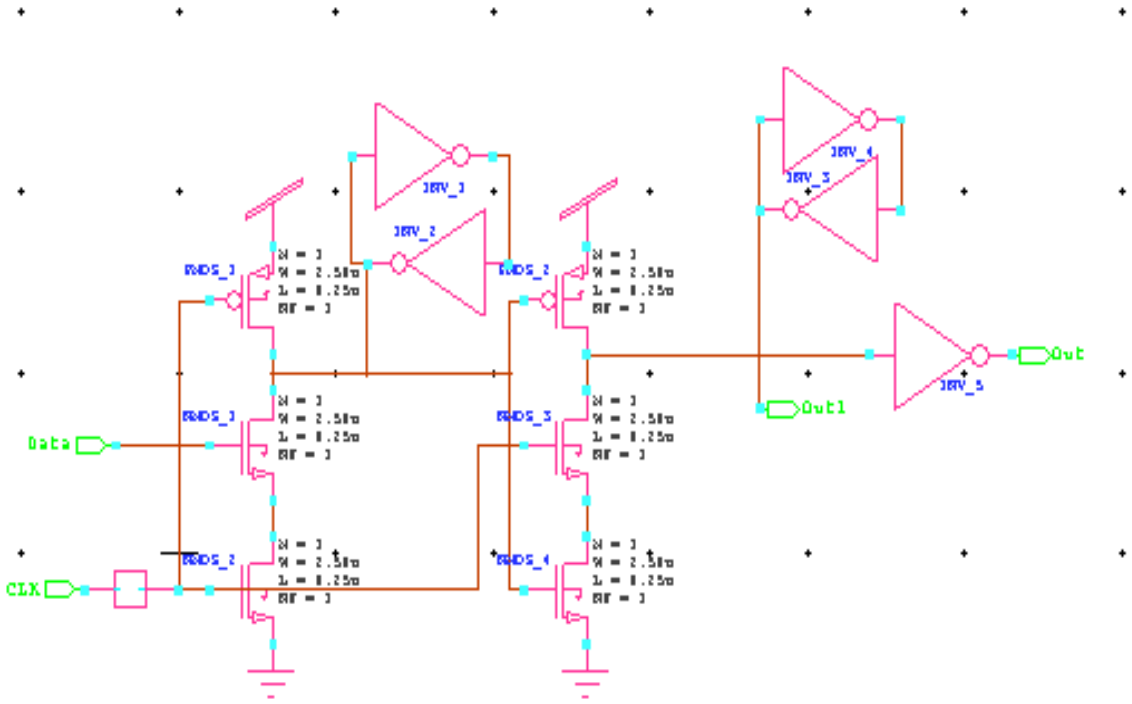

Fig: 1 ep-DCO

The pulse width is determined by the delay of three invertors. This design suffers from a serious drawback, i.e. ,the internal node X is discharged on every rising edge of the clock in spite of the presence of a static input "1".This gives rise to large switching power dissipation. To overcome this problem, many remedial measures such as conditional capture, conditional precharge, conditional discharge and conditional pulse enhancement scheme have been proposed [14]-[18].

B. Conditional discharge Flip-Flop

In this design the extra switching activity is eliminated by controlling the discharge path when the input is stable high and thus the name conditional discharge technique. When the input undergoes a LOW to HIGH transition the output Q changes to HIGH and QB to LOW. This transition at the output switches off the discharge path of the first stage to prevent it from discharging or doing evaluation in succeeding cycles as long as the input is stable HIGH. AN extra NMOS transistor controlled by the output signal

Q_fdbk is employed so that no discharge occurs if the input data remains "1".Power consumption in this design is high and the discharging path delay is more.

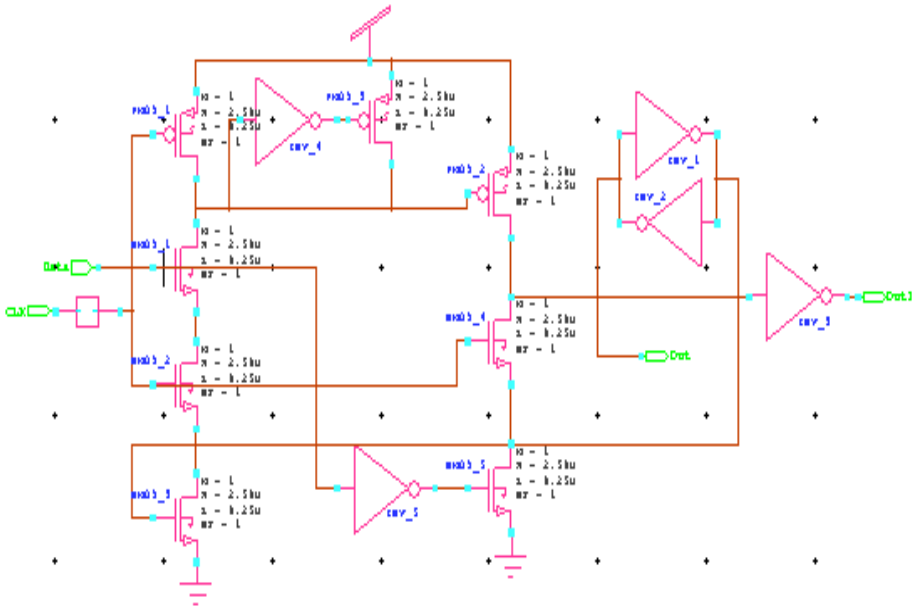

Fig: 2 conditional discharge flip-flop

C. Explicit type-Static Flip-flop

The schematic diagram of static type is presented in Fig.3.The ep- SFF reduces the switching activity by eliminating precharging node thus reducing power consumption. The internal node follows input during the sampling period. During the transparent period M3 and M6 turn on and the input is propagated to output.

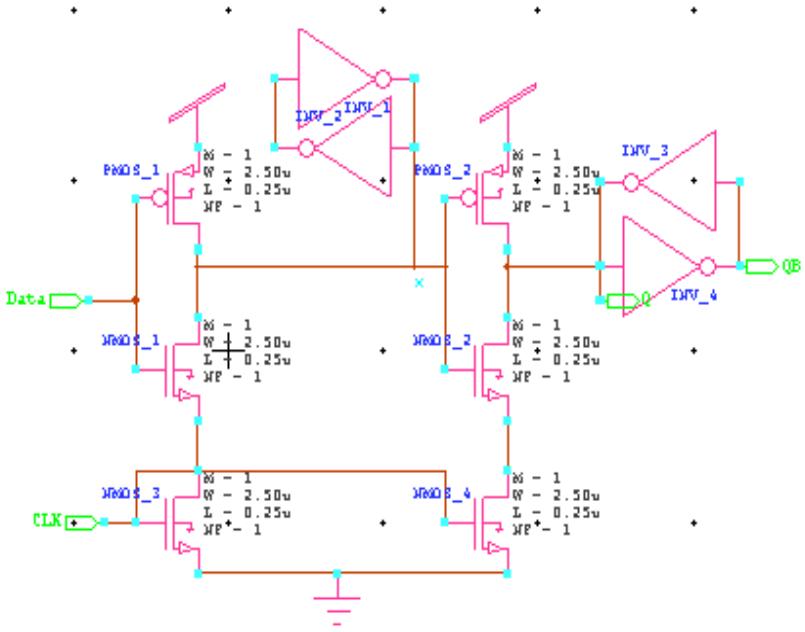

Fig: 3 ep- SFF

D. Conditional pulse enhancement scheme

This technique is devised to speed up the discharge along the critical path. In this paper, a novel low-power pulse-triggered flip-flop (FF) design is presented. First, the pulse generation control logic, and function, is removed from the critical path to facilitate a faster discharge operation. A simple two-transistor and gate design is used to reduce the circuit complexity. Second, a conditional pulse-enhancement technique is devised to speed up the discharge along the critical path only when needed. As a result, transistor sizes in delay inverter and pulse-generation circuit can be reduced for power saving.

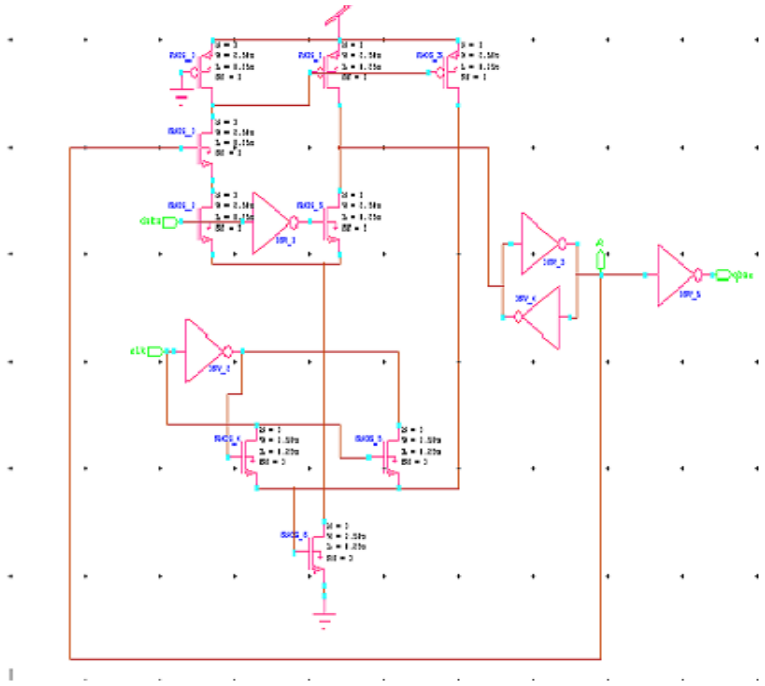

Fig 4: conditional pulse enhancement scheme

E. Proposed P-FF design

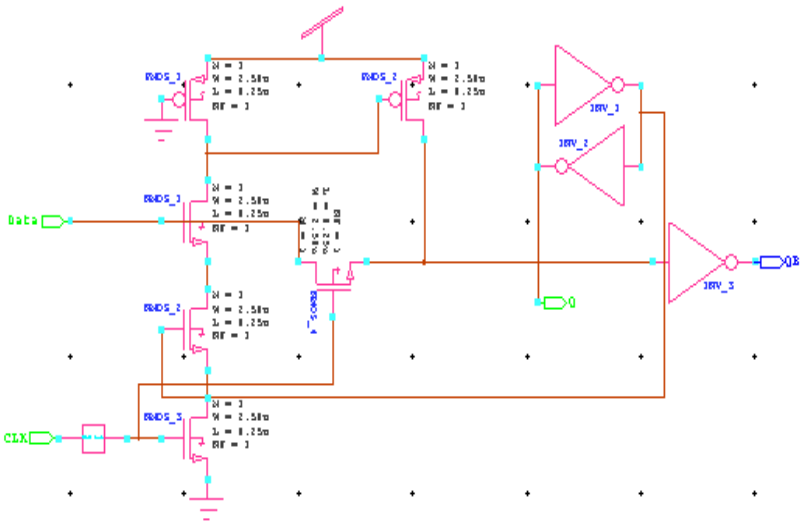

Fig 5: proposed flip flop design

This design adopts a signal feed-through technique to improve the delay at the critical path. This design employs a static latch structure and a conditional discharge scheme to avoid superfluous switching activity at the internal node. A weak pull-up p-MOS transistor with gate connected to the ground is used in the first stage of the TSPC latch. This gives rise to a Pseudo-n-MOs logic style design, and the keeper circuit for the internal node X can be saved. In addition to the circuit simplicity, this approach also reduces the load capacitance at node X.A pass transistor MNx controlled by the pulse clock is included so that input data can drive node Q of the latch directly. The operation of the proposed design is as follows. When a clock pulse arrives, if no data transition occurs, i.e., the input data and node Q are at the same level, on current passes through the pass transistor, which keeps the input stage of the FF from any driving effort. At the same time, the input data and the output feedback assume complementary signal levels and the pull-down path of node X is off. Therefore no signal switching occurs in any internal nodes, on the other hand, if "0" to"1" data transition occurs, node X is discharged to turn on transistor MP2, which then pulls node Q high.

III. Simulation Results

The performance of proposed P-FF design is evaluated against existing design through pre layout simulations. With regard to the latch structures, every P-FF is design is individually optimized subject to the product of power and D-to-Q delay.

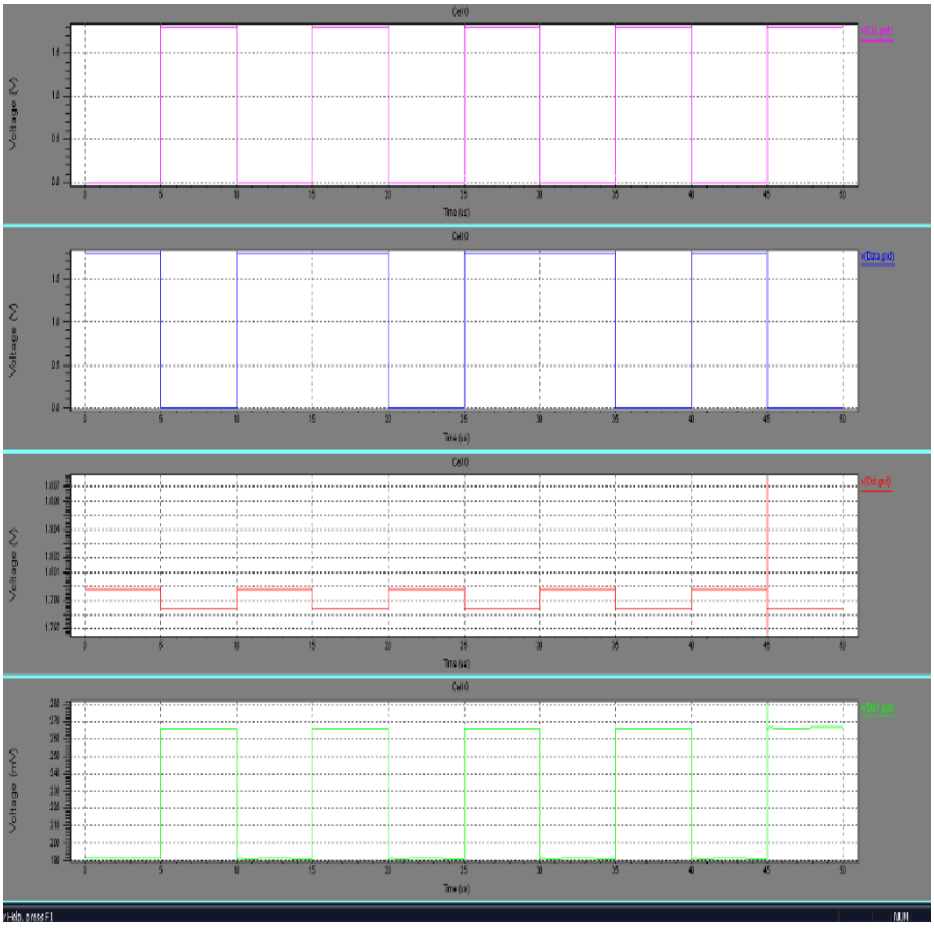

Fig 6 : waveform of ep-DCO

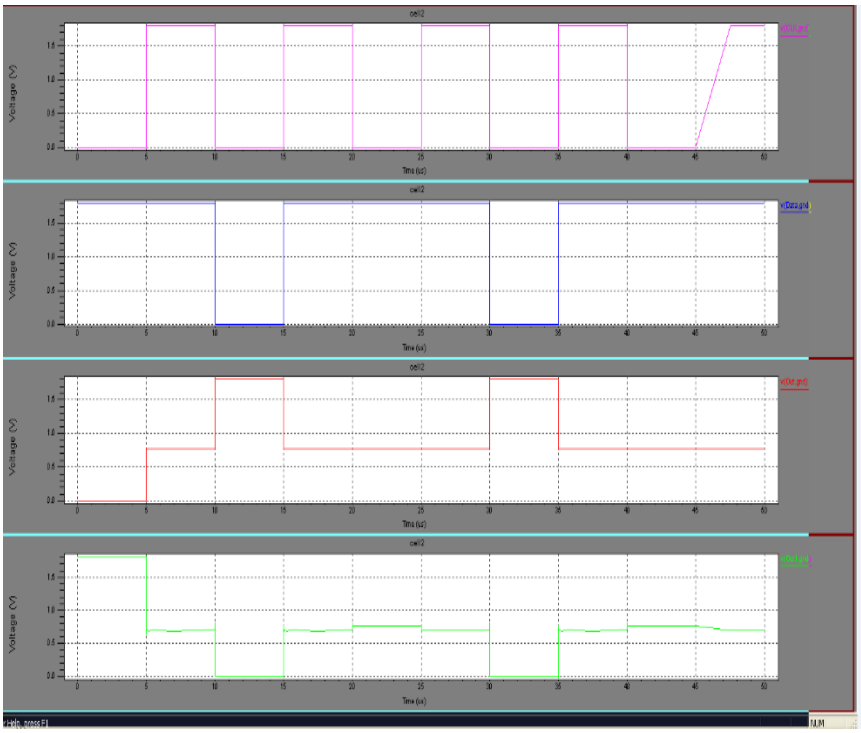

Fig 7: waveform of conditional discharge Flip Flop

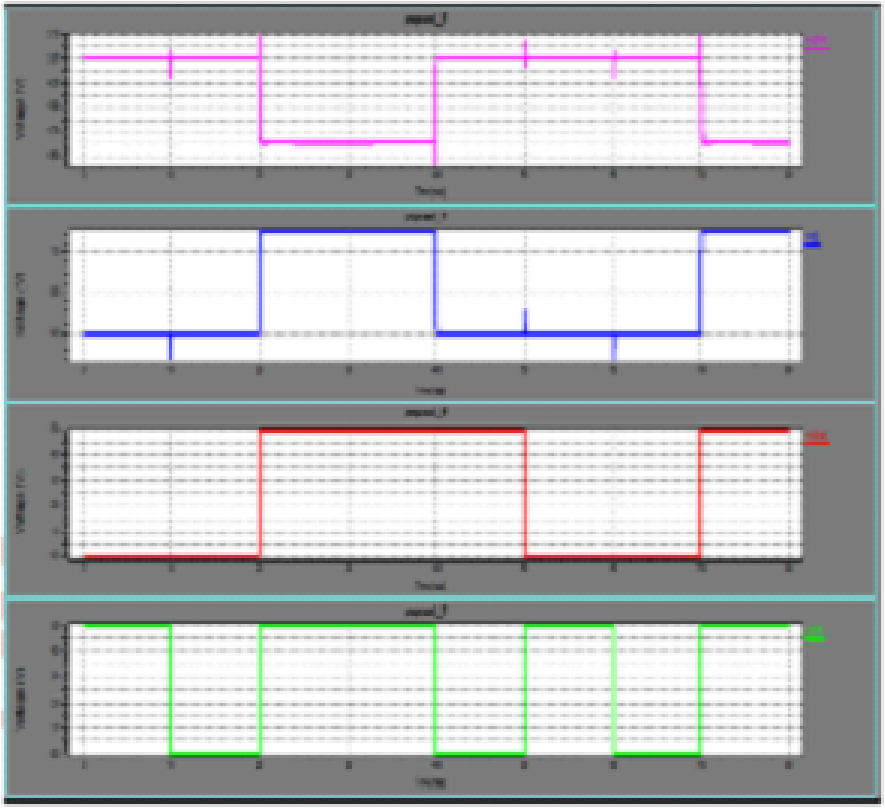

Fig 8: waveform of explicit type static flips flop

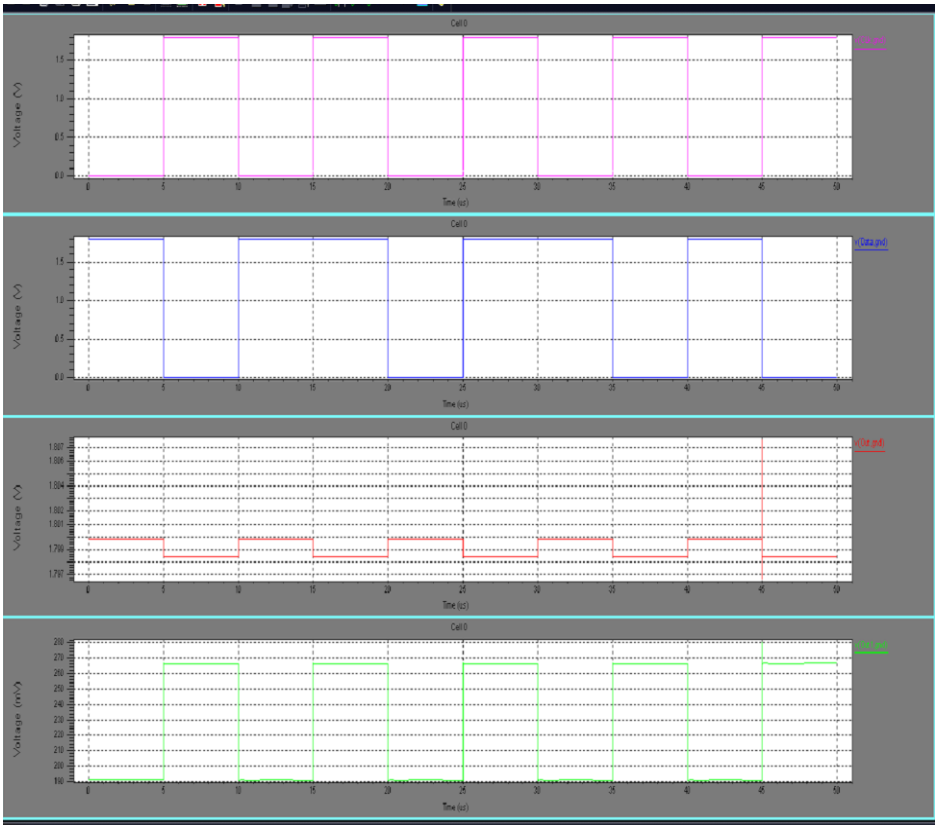

Fig 9: waveform of conditional pulse enhancement scheme

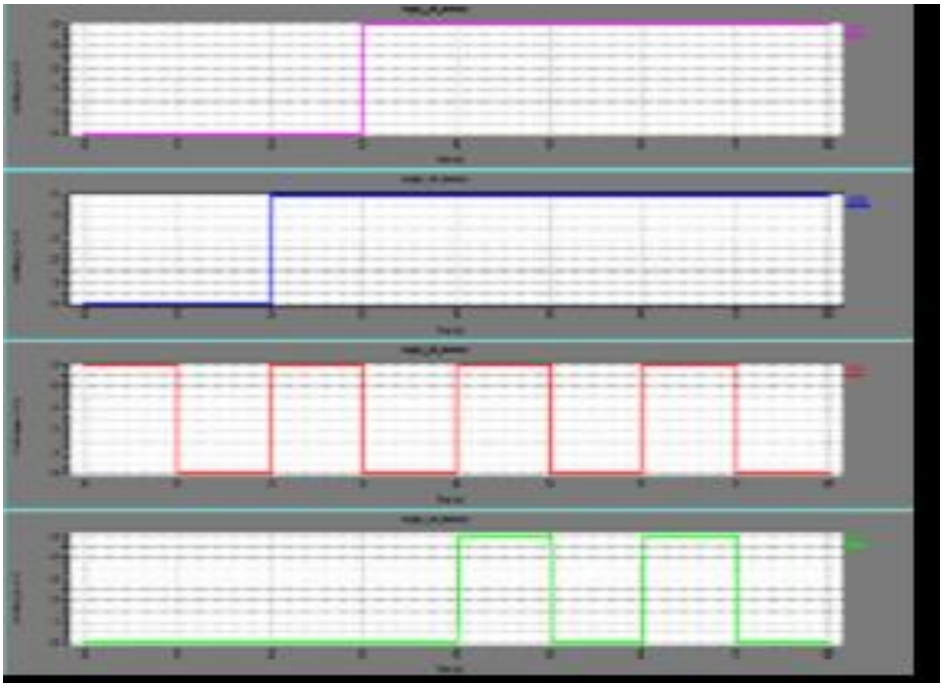

Fig 10: waveform of proposed technique

Table of Comparison:

FF designs	Ep-DCO	CDFF	Ep-SFF	Conditional pulse enhancement scheme	Proposed Technique
Number of transistors	28	30	14	19	12
Delay(ps)	118.9	129.5	145	107.24	182.4
Average power(μW)	34.41	34.08	71	31.11	30.09
Optimal PDP(pJ)	3.03	2.72	8.9	2.65	2.13

IV. Conclusion

In this brief, we presented a novel P-FF design by employing a modified TSPC structure incorporating a mixed design style consisting of a pass transistor and a pseudo-n-MOS logic. The key idea was to provide a signal feed through from input source to the internal node of the latch, which would facilitate extra driving to shorten the transition time and enhance both power and speed performance.

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