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RESEARCH ARTICLE

64 Bytes Cell Sized Distributed Packet Buffers for High-Bandwidth Routers

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Abstract* — Performance based routers rely on optimized packet buffers that support multiple queues and provide large capacity and short response time by combining hierarchical buffer architectures of SRAM/DRAM to meet performance based challenges but these architectures suffer from either larger SRAM requirement or higher time-complexity in the memory management. In this paper we propose a scalable and novel 64 bytes distributed packet buffer architecture which resolves the fundamental issues such as how to minimize the overhead of an individual packet buffer and how to design scalable packet buffers that uses independent buffer subsystems for which we first designing an efficient compact buffer that reduces the SRAM size requirement by (n(n-1))/2 and then we introduce a feasible way of coordinating multiple subsystems with a load-balancing algorithm that maximizes the overall system performance which are proved in both theoretically and with practical experimental results that demonstrates our load-balancing algorithm and the distributed packet buffer architecture can be easily scaled to meet the buffering needs of high performance bandwidth links and satisfy the requirements of scaling and support for multiple queues.

***Keywords*— Congestion SRAM, DRAM, Packet, Buffer, Router, Bandwidth**

I. Introduction

Now a day's almost everyone is using Internet to their best extent which intern increases the network traffic where 70% are male users and 30% are female users according to the resent survey being conducted online. Over the Internet a user makes use of the current trends of communication link bandwidth where routers play a crucial role in sustaining this growth by being able to switch packets extremely fast to keep up with the growing bandwidth and due to this demands sophisticated packet switching and buffering techniques a packet buffer need to be designed to supports maximum capacity with implementation of multiple queues and provide short response time.

The main component of any router is its buffer and the main characteristic of it is its capacity or size and speed of switching the packets in resent past years routers came up with buffer which is a temporary memory where the whole work of a router is being done that is RTT*LR [3] data, where RTT is considered a round trip time for data packets that pass through a router and LR is Line Rate. We size of the router buffer is considered to be the backbone of a router which can be reduced at the expense of a small loss in throughput since the out flow and the inflow capacity ratio of a network link mostly determines the required buffer size of a router which is limited in size the more the size of buffer the more is the network traffic capacity and less congestion, but if the buffer size is less the congestion creation is more but less power deception. So we need to consider both the cases and need to design correct sized buffer depending on the expected usage of it.

The algorithm which we preferred over the many algorithms that have been proposed in this area is Best Grained IP base quality of service where a router buffer usually maintains thousands of packet queues for example Ali-series routers maintain as many as 128,000 queues of data packets but many of us desire a packet buffer that supports millions of queues but not only that a packet buffer should be capable of sustaining continuous streams of data in the form of inflow and outflow with inbound and outbound capacity due to ever increasing line rate with increase in internet speeds and bandwidth capacity for cheaper cost, memory technologies such as SRAM or DRAM alone cannot reach the requirements of on-demand technology.

In this paper we propose packet buffer architecture that present scalable and efficient hierarchical packet buffer architecture that combines the SRAM occupancy which has been significantly reduced with the advantage of parallel DRAM, we first propose Random Round Robin (RRR) memory management algorithm which is based on the traffic based approach that aims to provide different services for different types of data streams where the proposed architecture reduces the size of SRAM by more than 96 percent and the maximal delay when the traffic intensity is increased over 70%.

The below figure 1 contains the basic architecture of a router that performs manly two tasks first one is to run routing algorithms or protocols such as RIP, OSPF, BGP and the second one is switching datagrams or packets from incoming to outgoing link.

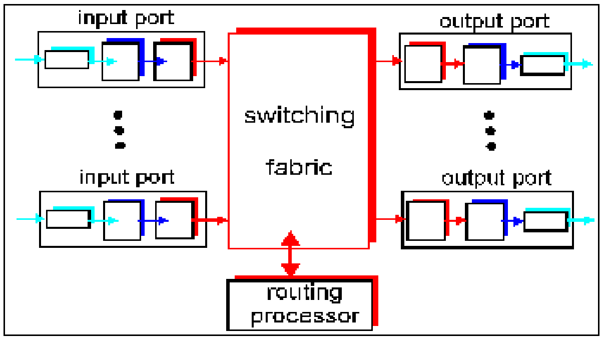


Fig. 1 Basic Architecture of a Router.

II. LITERATURE SURVEY

Random-access memory-RAM is a device that allows data items to be read and written in roughly the same amount of time regardless of the order in which data items are accessed and is in the form of integrated circuit and is a volatile types of memory where the stored information is lost if the power is removed and one of such type of RAM is a Static Random Access Memory-SRAM is a type of semiconductor memory that uses latching circuitry to store each bit of data and the other type of RAM is Dynamic RAM-DRAM must be periodically refreshed but both the memories are considered to be volatile.

Access time is a major characteristic with respect to a router buffer but SRAM and DRAM cannot individually meet the access time and capacity requirements of router buffers where as SRAM is fast enough with an access time of around 2.5 ns but its largest size is limited by current technologies to only a few MB where as a DRAM can be built with large capacity and the memory access time is around 40 ns which is very huge compared to SRAM [2]. Over the last decade the memory access time of DRAM is decreased by only 10 percent every 18 months but our proposed system need to have high speed buffer and according to a recent survey the line-rate is increased by 100 percent every 18 months, in order to keep the DRAM modules busy we need to transfer a minimum size chunk which in other words is called as blocking of data into it to effectively utilize the available bandwidth provided by the DRAM module.

To conduct a quantitative analysis on ratio access time between the DRAM and SRAM we need to check access granularity of DRAM say b times that of the SRAM but the access time alone cannot determine the access granularity but we need to also consider on the bandwidth, and the frequency where the SRAM is twice that of the

DRAM but the odd situation also happens when a DRAM with shorter access time and higher bandwidth is introduced but there is no guarantee that the speed mismatch is improved. And the next problem is if our architecture has multiple SRAM and DRAM devices then it becomes meaningless to compare the access time of individual memory devices and even worst problem arose when the allowed minimal access granularity of SRAM is less than the cell size.

We came up with an approach of designing packet buffers such that we maintain multiple queues instead of a single FIFO queue by which we can dispatching and store packets in multiple separate queues instead of single which is considered to be a major overhead of all the memory management algorithms. Here we have designed a packet buffer to find an efficient way to bridge the gap of size between the memory cell and the memory chunk that bridges the gap of SRAM access time and DRAM storage capacity and hence forth creating a large scale multiple queuing techniques.

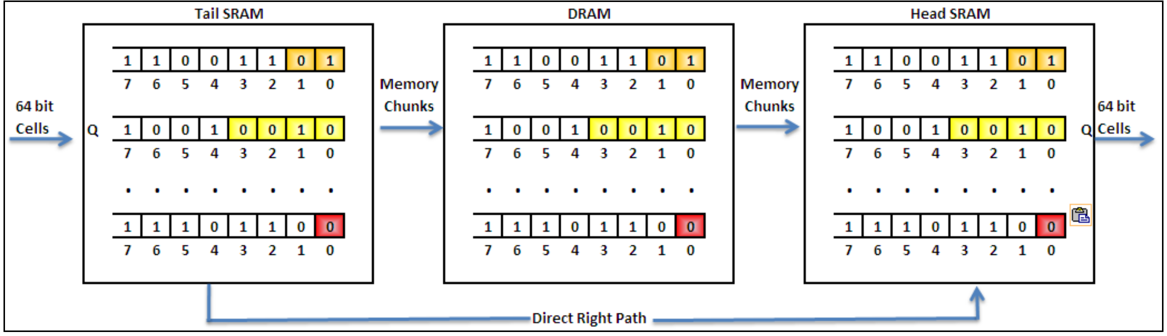


Fig. 2 Proposed Architecture

In the above figure 2 we introduced the basic hybrid architecture of SRAM/DRAM with one DRAM sandwiched between two smaller SRAM memories where the two SRAMs hold heads and tails of all the queues and on the same hand DRAM maintains the middle part of the queue the architecture is designed such a way that it simply shuffles data packets between SRAM and DRAM is performed by the memory management algorithm which holds the amount of data for each queue in both the inflow and outflow of SRAM so as to change the scattered DRAM accesses into a continuous one because we know that the batch loads are strictly limited within each queue.

III.PROPOSED SYSTEM

We can perform write and read operations in SRAM or DRAM one after other or simultaneously, suppose a FIFO queue accumulates a specific amount of data say k is transferred to the DRAM through a single write operation and if suppose 2 write operations of k size is performed on queue then the situation may guarantees a queue overflow or in other words queue may be considered to be full. So in order to handle such situation of queue overflow we need to use the concept of pipelining or else we need to use the algorithm called as Earliest Critical Queue First (ECQF) which reduces the size of over head on SRAM by 1 with the creation of an extra delay which is again an overhead.

A 64 bytes DRAM is utilized in this architecture since in certain family of DRAM the chunk size of k bytes is determined by two factors: bandwidth and its typical memory access time, in order to meet the speed of SRAM we need to utilize multiple slower DRAM's instead of one DRAM with same bandwidth by which multiple queues can be accommodated and then the memory management algorithm is responsible for distributing the data between k queues which can be arbitrated using a bipartite graph for maximum matching[1] problem.

One of the major task for us is to designing a general-purpose packet buffer for a specific application where buffer behavior is predictable and by which a task can be greatly simplified and the proposed memory architecture is applicable to both the packet buffering problem as well as the various network flow states that are implemented and the same data could potentially be read for several times and however this architecture assumes perfect randomization while performing the requests to the memory banks which may lead to the buffer overflow and start dropping requests which intern degrades the system performance.

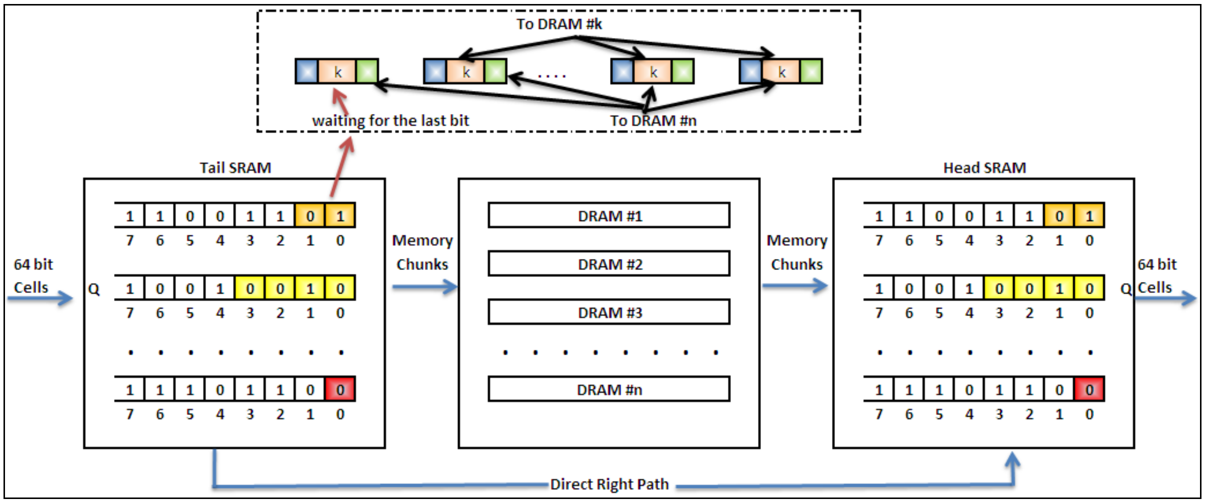


Fig. 3 Buffer Behavior in our proposed architecture with multiple DRAMs.

As shown in above Fig. 3, the DRAM structure is the extend version of above mentioned structure in Fig 2, where we implemented as a combination of n DRAMs that simply provides a data bus of width k times that of a single DRAM data bus with a fixed chunk size of a single DRAM, here in the proposed architecture the scale of batch load is being increased because we implanted queues to maintain huge size of data by accumulating it at once which allows us to perform write operations into DRAM using a mutual data bus by which the size gap between cell and chunk is being compromised.

The working nature of the proposed architecture is we have given only the first 64 bytes of data that arrived into a queue and then data stayed in the SRAM infinitely because the SRAM size is selected such that it can easily accommodate more than 64 Bytes. Then the departure time of each chunk relies on the corresponding traffic pattern and more over the currently available DRAMs are around 64 to 320 bytes of size and the data is arrived in each of the multiple queues and an unbalanced traffic allocation is created among the DRAMs that is only the first DRAM receives all the data of 64 bytes. But to achieve long-term output balance we need to implement per-queue Round Robin scheme but even though the short-term biased output still exists since the heads of currently active queues in the output may all be allocated to a particular DRAM which leads to a bottleneck of entire system.

IV. Simulation Results

We simulated the proposed architecture of a compact packet buffer with 10 DRAMs based on 64 Byte cells and the results obtained are shown below.

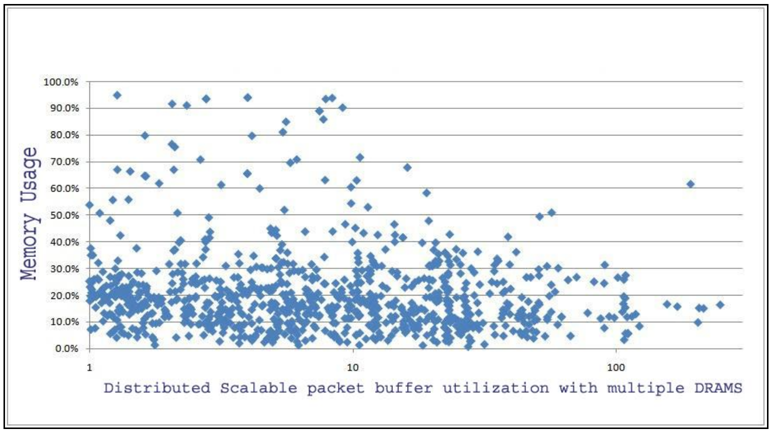


Fig. 4 Distributed scalable packet buffer utilization

The above figure 4 we have simulated in the data mining environment using a open source tool by name Weka3.6 where the plotted chart represents the utilization of the DRAM and 100% utilization is being achieved very less.

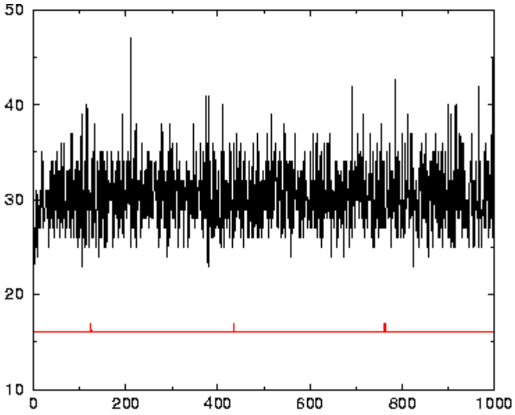
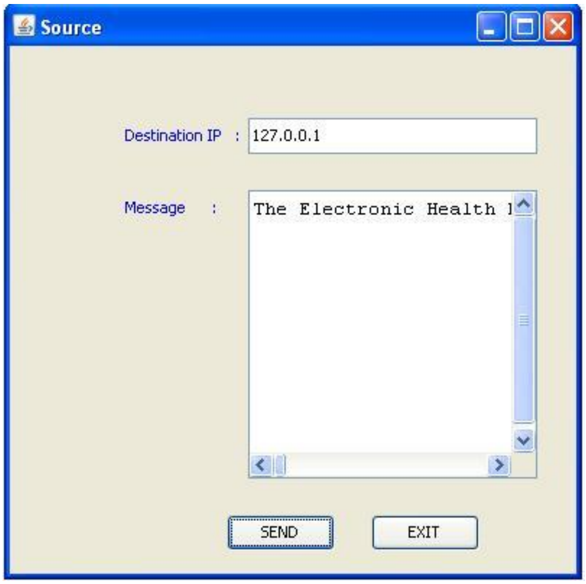


Fig. 5 System performance under proposed architecture.

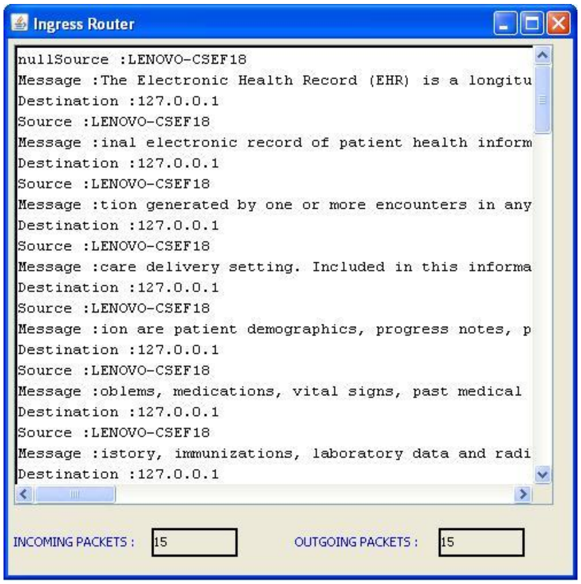
In the above figure 5 the system performance is ranging between 25 to almost 35 at the scale of 0 to 50 which if we scale from 0 to 100 we need to double the value which generates higher hypothesis and will show a better performance. And we have implemented our proposed system in java and some of the screens are:



Destination IP : 127.0.0.1

Message : The Electronic Health I

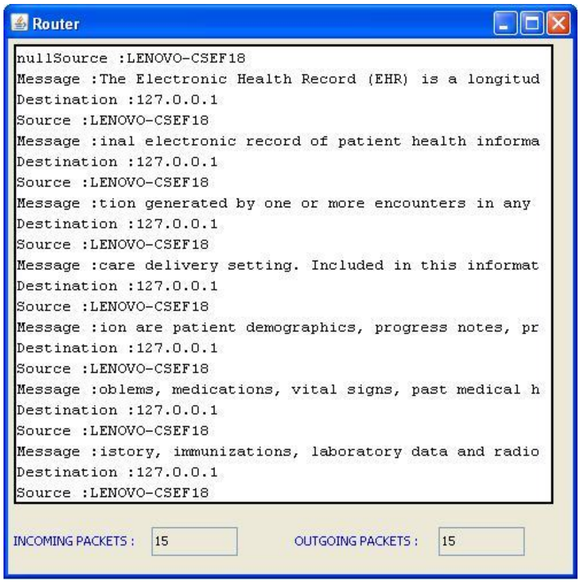
Fig. 6 depicting destination IP address and the message to be sent to it.



```
nullSource :LENOVO-CSEF18
Message :The Electronic Health Record (EHR) is a longitu
Destination :127.0.0.1
Source :LENOVO-CSEF18
Message :inal electronic record of patient health inform
Destination :127.0.0.1
Source :LENOVO-CSEF18
Message :tion generated by one or more encounters in any
Destination :127.0.0.1
Source :LENOVO-CSEF18
Message :care delivery setting. Included in this informa
Destination :127.0.0.1
Source :LENOVO-CSEF18
Message :ion are patient demographics, progress notes, p
Destination :127.0.0.1
Source :LENOVO-CSEF18
Message :oblems, medications, vital signs, past medical
Destination :127.0.0.1
Source :LENOVO-CSEF18
Message :istory, immunizations, laboratory data and radi
Destination :127.0.0.1
```

INCOMING PACKETS : 15   OUTGOING PACKETS : 15

Fig.7 Status of Ingression Router.



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nullSource :LENOVO-CSEF18
Message :The Electronic Health Record (EHR) is a longitud
Destination :127.0.0.1
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Message :inal electronic record of patient health informa
Destination :127.0.0.1
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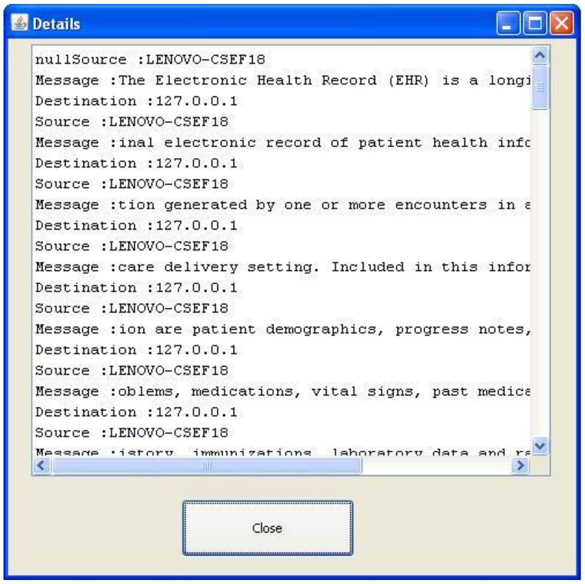
Message :oblems, medications, vital signs, past medical h
Destination :127.0.0.1
Source :LENOVO-CSEF18
Message :istory, immunizations, laboratory data and radio
Destination :127.0.0.1
Source :LENOVO-CSEF18
```

INCOMING PACKETS : 15   OUTGOING PACKETS : 15

Fig. 8 Router status with 15 incoming and outgoing packets.



```
nullSource :LENOVO-CSEF18
Message :The Electronic Health Record (EHR) is a longi
Destination :127.0.0.1
Source :LENOVO-CSEF18
Message :inal electronic record of patient health infc
Destination :127.0.0.1
Source :LENOVO-CSEF18
Message :tion generated by one or more encounters in a
Destination :127.0.0.1
Source :LENOVO-CSEF18
Message :care delivery setting. Included in this infor
Destination :127.0.0.1
Source :LENOVO-CSEF18
Message :ion are patient demographics, progress notes,
Destination :127.0.0.1
Source :LENOVO-CSEF18
Message :oblems, medications, vital signs, past medica
Destination :127.0.0.1
Source :LENOVO-CSEF18
Message :istory, immunizations, laboratory data and ra
```

Fig. 9 Log file of complete transmission of packets.

V. CONCLUSION

In this paper we have came up with construction of packet buffers architecture that is based on a hybrid SRAM/DRAM while introducing minimum overhead is the major issue discussed in this paper and we also increased the throughput and storage capacity of a packet buffer by implementing parallel mechanism on multiple DRAM chips and also we proved that the previous algorithms make very little effects in exploring the advantage of parallel DRAMs leading to the requirement of large size of a SRAM and high time complexity in memory management. We also proposed novel packet buffer architecture which uses both fast batch load scheme and a hierarchical distributed structure by reducing the requirement of SRAM size at the maximum and also we have shown the results which are generated using java1.5 which indicates that the proposed architecture guarantees performance in terms of the low time complexity with short access delay.

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