Available Online at www.ijcsmc.com

International Journal of Computer Science and Mobile Computing

A Monthly Journal of Computer Science and Information Technology

ISSN 2320–088X

*IJCSMC, Vol. 2, Issue. 4, April 2013, pg.455 – 466*

RESEARCH ARTICLE

# DESIGN AND ANALYSIS OF POWER EFFICIENT CLOCKED PAIR SHARED FLIP FLOP

**B. Ragavi[1], K. Rajesh[2], A. Selvapandian[3]**

[1]Final Year, M.E (Applied Electronics), Department of Electronics and Communication Engineering, R.V.S CET, Dindigul, India

[2]Assistant Professor, Department of Electronics and Communication, RVS CET Dindigul, India

[3]Assistant Professor, Department of Electronics and Communication, PSNACET, Dindigul, Tamilnadu, India

*[1] ragavi2christ@gmail.com; [2] krajeshk1980@rediffmail.com; [3] selva6040@gmail.com*

***Abstract— In this paper, we examine the problems in the CDN of the flip flop & design an improved CDN oriented Flip-flop which is Clocked Pair Shared Flip Flop (CPSFF). Clock Division Network (CDN)'S plays an important role in the flip flop design and it's the major element in the flip –flop for producing the logical outputs it's much important to design the CDN with low power and area. Power consumption is the main traffic jam of system performance. Low power flip-flops which plays a vital role for the design of low-power digital systems. Flip flops and latches consume a large amount of power due to redundant transitions and clocking system. In addition, the energy consumed by low skew clock distribution network is steadily increasing and becoming a larger fraction of the chip power. Almost, 30% - 60% of total power dissipation in a system is due to flip flops and clock distribution network. In order to achieve a design that is both high performances while also being power efficient, careful attention must be paid to the design of flip flops and latches. We survey a set of flip flops designed for low power and High performance.***

***Key Terms: - Flip Flop; Clock Division Network; Clocked Pair Shared Flip Flop; Power***

## I. INTRODUCTION

In the long-ago, the main concerns of the VLSI designer were area, performance, cost and consistency. Power reflection was frequently of only secondary importance. In modern years, however, this has begin to change and, more and more, power is being given similar weight to area and speed consideration. One of the vital factors is that too much power utilization is becoming the limiting factor in integrating additional transistors on a single chip or on a multiple-chip module. Except power consumption is considerably summary, the resulting heat will limit the feasible packing and performance of VLSI circuits and systems. Most of the current designs are synchronous which implies that flip-flops and latches are involved in one way or another in the data and control paths. One of the challenges of small power methodologies for synchronous systems is the power consumption of the flip-flops and latches. It is important to save power in these flip-flops and latches without compromising state integrity or performance. Power Consumption is dogged by some factors as well as frequency f, supply voltage, data activity, capacitance, leakage and short circuit current.

$$P = P_{dynamic} + P_{short\ circuit} + P_{leakage} \rightarrow (1)$$

On top of equation Pshort circuit is the short circuit power which is caused by the finite rise and fall time of input signals, resulting in both the pull up network and pull down network to be ON for a short period. Pdynamic is called the switching power .P leakage current= I leakage*Vdd.

This paper surveys Flip Flop comparison metrics in II,. After that we detailed on the survey of existing methods III, then we propose a novel clocked pair shared flip- flop in Section IV. Section V presents simulation results. Section VI concludes this paper.

## II. FLIPFLOP COMPARISON METRICS

There are a number of fundamental performance metrics that are used to qualify a flip-flop and evaluate it to other designs.

### A. Clock-to-Q delay

Propagation delay from the clock input to the output Q terminal. This is assume that the data input D is set early enough with respect to the useful edge of the clock input signal.

### B. Setup time

The least amount time wanted among the D input signal modify and the triggering clock signal edge on the clock input. This metric guarantee that the output will chase the input in bad case conditions of process, voltage and temperature (PVT). This assumes that the clock triggering edge and pulse have enough time to detain the data input change.

### C. Hold time

The smallest amount time needed for the D input to stay stable after the occurrence of the triggering edge of the clock signal. This metric guarantees that the output Q stays stable after the triggering edge of the clock signal occurs, under worst PVT conditions. This metric assumes that the D input change happened at least after a minimum delay from the previous D input change.

### D. Data-to-Q delay

The addition of setup of data to the D input of flip-flop and the Clock-to-Q delay as defined above. Knowing that flip-flops are forever in the critical path of a synchronous design standard cell library developers always try their best to minimize the setup time requirement of flip-flops and the Clock-to-Q delay to target the highest possible frequency for the design at hand. Grasp times are not as critical as setup times and they do not impose an upper bound on the speed of a circuit in flip-flop based designs.

On the other hand they are very serious in latch-based designs.

1. Stable region

Where the setup and hold times of a flip-flop are met and the Clock-to-Q delay is not dependent on the D-to-Clock delay. This is the required region of operation.

2. Metastable region

As D-to-Clock delay decreases, at a certain point the Clock-to-Q delay starts to rise exponentially and ends in failure. In this section, the Clock-to-Q delay is nondeterministic causing alternating failures and behaviors which are very difficult to debug in real circuits not to mention silicon.

3. Failure region

Where changes in data are unable to be transferred to the output of the flip-flop. The best setup time noted on the graph would be the highest performance D-to-Clock delay to finish fastest D-to-output delay. Due to the steep curve to the left of that point not all library developers would target this value. Fig.1. shows an optimal setup time for D-toClock.

## III. SURVEY OF EXISTING METHODS

Most of the flip-flops presented now are dynamic in nature, and some internal nodes are precharged and evaluated in each cycle without producing any useful activity at the output when the input is stable. Reducing this redundant switching activity has a profound effect in reducing the power dissipation, and in the literature many techniques were presented for this purpose [8]–[13]. A brief survey of such techniques is conducted in this work, and the main techniques were classified as follows:

### A. CONDITIONAL CAPTURE FLIP FLOP

Conditional Capture [14] technique is proposed for disabling redundant internal transitions. This technique achieves significant power reduction at little or no delay penalties. Motivation behind Conditional Capture [14] technique is the observation that considerable portion of power is consumed for driving internal nodes even when the value of the output is not changed (corresponding to low input activities). It is possible to

disable internal transitions when it is detected that they will have no effect on output. But the drawback is increased set-up time for sampling zero (low level) and also heavier load is presented to the Q output of the flip flop.

B. CONDITIONAL PRECHARGE FLIP FLOP

For overcoming the difficulty in Conditional Capture Flip Flop[14], Conditional pre-charge flip flop[15] is proposed . One of the most vital assistance of this work is associated to preventing unconditional pre-charge operation of the internal node, strongly linked to too much power dissipation of the circuit. This is skilled by scheming the return of internal node to inactive (high) state, allowing the internal node to stay at low level until input condition is changed. This approach powerfully eliminates the unnecessary transitions of the internal node as well as race condition at the output. There are two main disadvantages: One is introducing another critical path for low input level capture. Another drawback is increasing the output load due to the feedback, which although minimal size transistor can be used, being out of the critical path, can have an effect on whole propagation holdup.

C. CONDITIONAL DISCHARGE FLIP FLOP

Conditional Discharge Flip-flop (CDFF)[10] not only reduce the interior switching actions, other than also generates fewer glitches at the output, while maintaining the negative setup time and small Q-to-output delay characteristics as shown in fig 4. With a data-switching activity of 37.5%, this flip-flop can save up to 39% of the energy with the equal speed. In this Flip-flop, the extra switching activity is eliminated by scheming the ejection path when the input is stable HIGH. In this scheme, an n-MOS Transistor is inserted in the discharge path with the high-switching activity. When the input undergoes a LOW-to-HIGH transition, the output changes from HIGH to LOW. This transition at the output switches sour.

D.CONDITIONAL DATA MAPPING FLIP-FLOP (CDMFF):

Conditional Data Mapping Flip flop[8] used just seven clocked transistors, resulting in about50% reduction in the number of clocked transistors , for this reason CDMFF used less power than CCFF[14] and CDFF[10] . Note that CDFF used double edge clocking. For ease purposes, we did not include the power savings through double edge triggering on the clock distribution network. This shows the effectiveness of reducing clocked transistor numbers to achieve low power, Since CDMFF [8] outperforms CCFF and CDFF. But it makes very difficult to apply the Double edge triggering and also it cannot be used in a low swing environment. Moreover it reduces the number of clocked transistors but it has redundant clocking as well as floating node. So we can move into the clocked pair shared flip-flop.

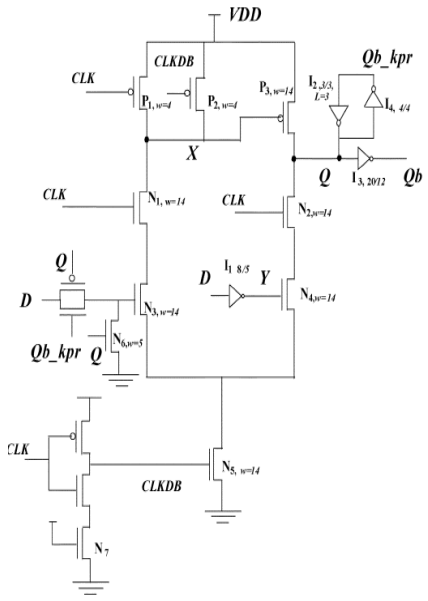



Fig .1 .CDMFF Flip-flop

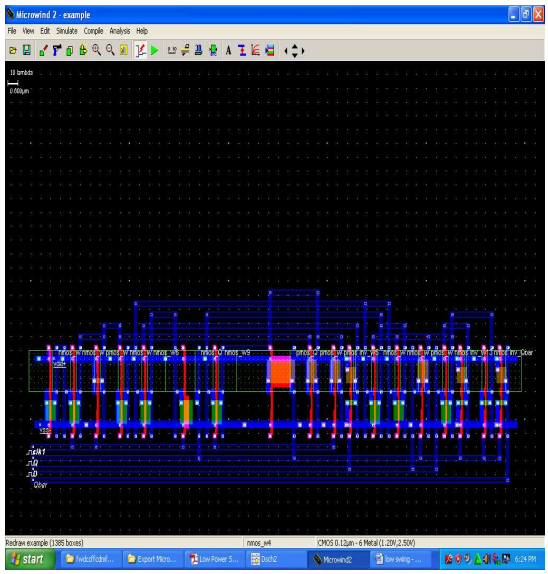
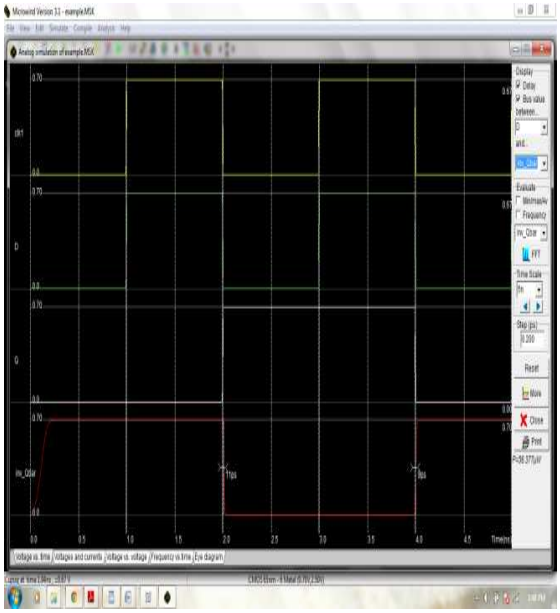


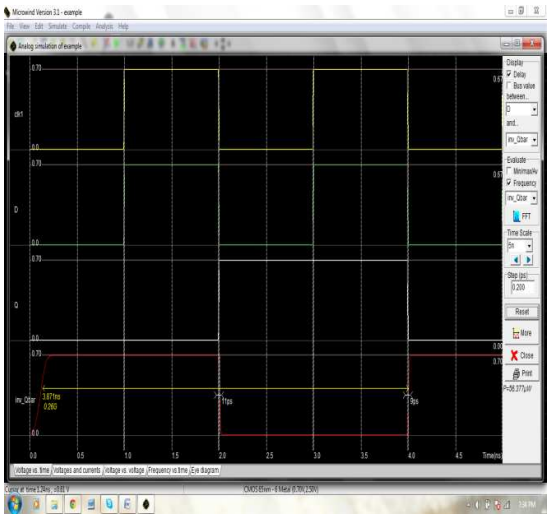
Fig .2. CDMFF layout in microwind



Power = 56.377uw

Fig.3.CDMFF output waveform with power consumption



Delay=3.871ns, Frequency= 258MHZ

Moreover it reduce the number of clocked transistors except it has redundant clocking as well as floating node. So we can go into the clocked pair shared flip-flop.

E.LOW-SWING DIFFERENTIAL CONDITIONAL CAPTURING FLIP-FLOP[LSDCCFF]

Low-swing differential conditional capturing flip-flop (LS-DCCFF)[1] operate with a low-swing sinusoidal clock during the operation of reduced swing inverters at the clock port. By means of a low-swing differential conditional capturing flip-flop (LS-DCCFF) for use in low-swing LC resonant CDNs. This is the first application of low-swing clocking to LC resonant CDNs. Low-swing clocking would normally require two voltage levels, These voltage levels can be generated using one of two schemes: 1) dual-supply voltages and 2) regular power supply. The first scheme adds circuit and extra area complexity to the overall chip design and layout.

Low swing voltage clock signals might be connected to then MOS transistors N3 and N4, respectively. In adding, it is easy to construct double edge triggering flip-flop based on the simple clocking structure in CPSFF. Additional CPSFF could be used as a level converter flip-flop automatically, because incoming clock and data signals only drive nMOS transistors.

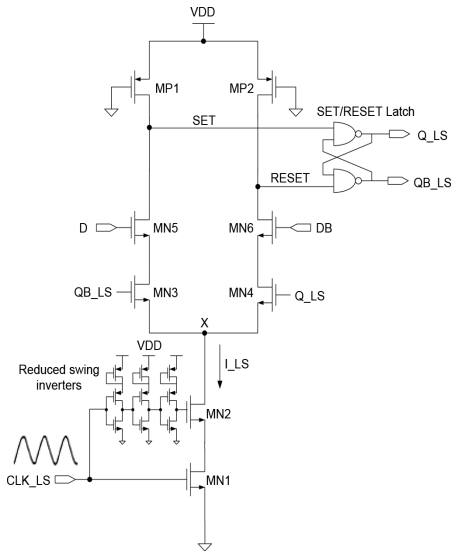



Fig .4. Low Swing Differential Conditional Capturing Flip Flop

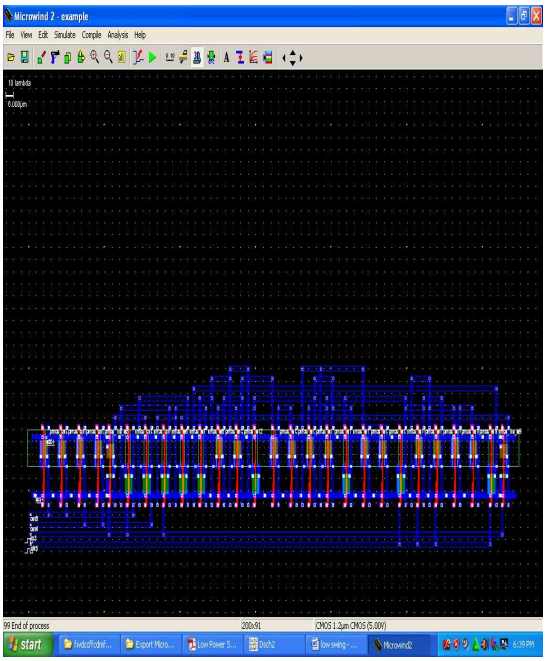
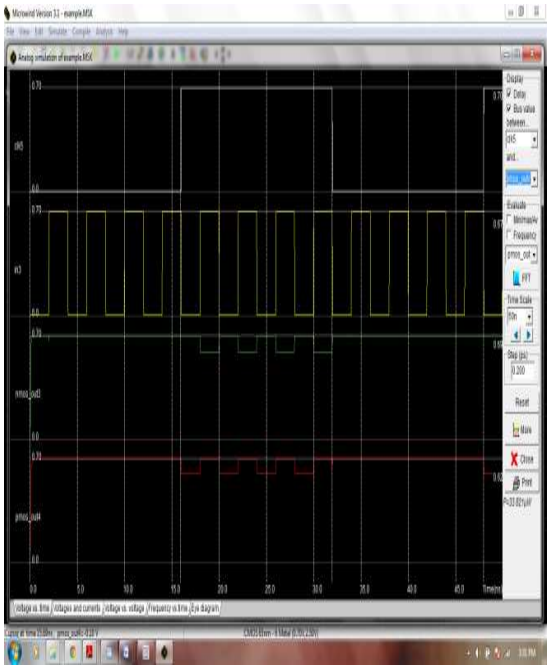


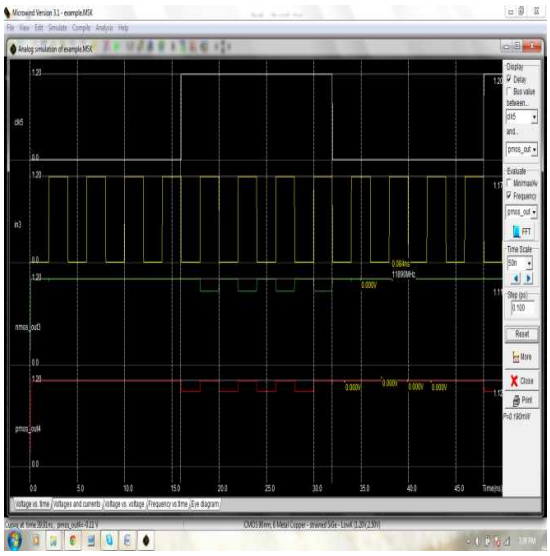

Fig.5.LSDCCFF Layout in microwind



POWER = 33.821 uw

Fig.6 LSDCCFF output waveform with power consumption



Delay=0.084ns, Frequency=59450MHZ

Amount of transistors are reduced in this method. But act is very poor in this method. So we are going to Clocked Pair Shared Flip flop.

## IV. PROPOSED CLOCKED-PAIR-SHARED FLIP FLOP

CDFF and CCFF use a set of clocked transistors. CDMFF reduces the amount of clocked transistors but it has redundant clocking as well as a suspended node. To ensure efficient and robust implementation of low power sequential element, we propose Clocked Pair Shared flip-flop(CPSFF) to apply a smaller amount clocked transistor than LSDCCFF and to overcome the floating difficulty in CDMFF .In the clocked-pair-shared flip-flop, clocked pair (N3, N4) is shared by first and second stage. An always on pMOS, P1, is used to charge the internal node rather than using the two clocked precharging transistors (P1, P2) In CDMFF. Evaluate with other methods, a whole of three clocked transistors are reduced, such that the clock load seen by the clock driver is decreased, resulting in an efficient design. CPSFF uses four clocked transistors somewhat than seven clocked transistors in CDMFF, resulting in about 40% reduce in number of clocked transistors. In count the inner node X is connected to Vdd by an always on P1, so X is not floating, resulting in improvement of noise robustness of node X. The always ON P1 is a weak pMOS transistor. This scheme combines pseudo nMOS with a conditional mapping technique where a feedback signals, *comp*, controls nMOS N1.

what time input D stays 1,Q=1, N5 is on, N1 will shut off to avoid the avoidable switching activity at node X as well as any short circuit current. pMOSP2 should pull Q up when D transits to 1. The second nMOS branch (N2) is dependable for pulling down the output of Q if D=0 and Y=1 when the clock pulse arrives. pMOS in I1 should turn on Nmos .

An amount of low power techniques can be easily incorporated into the new flip-flop. Unlike CDMFF and LSDCCFF, low swing is likely for CPSFF since incoming low voltage clock does not drive pMOS transistors.

Low swing voltage clock signals might be associated to then MOS transistors N3 and N4, respectively. In adding, it is easy to construct twice edge triggering flip-flop based on the simple clocking structure in CPSFF. Further CPSFF could be used as a level converter flip-flop mechanically, since received clock and data signals only make nMOS transistors.

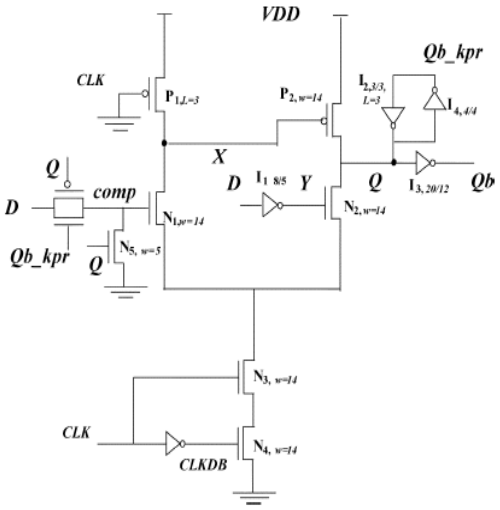



Fig .7.Clocked Pair Shared Flip Flop

Table I
Comparing the Flip-Flop in terms of No of
Transistors and No of Clock Transistor

| Flip Flops | No. of Transistors | No of Clock Transistors |
|---|---|---|
| CCFF | 26 | 13 |
| CPFF | 23 | 12 |
| CDFF | 28 | 15 |
| CDMFF | 22 | 7 |
| CPSFF | 19 | 4 |

## V. SIMULATION RESULTS

The simulation results obtained by means of Microwind and DSCH tool. The microwind program allows the student to propose and simulate an integrated circuit at physical description level. MICROWIND is really integrated EDA software encompassing IC designs from concept to completion, enabling chip designers to design beyond their mind. MICROWIND integrates traditionally separated front-end and back-end chip design into an integrated flow, accelerating the design cycle and reduced design complexities. It tightly integrates mixed-signal implementation with digital implementation, circuit simulation, transistor-level extraction and verification – providing an innovative education initiative to help individuals to develop the skills wanted for design positions in virtually every domain of IC industry.

The DSCH program is a logic editor and simulator. DSCH is use to confirm the architecture of the logic circuit previous to the microelectronics design is happening. DSCH provides a user-friendly environment for hierarchical logic design, and fast simulation with delay analysis, which allows the design and validation of complex logic structures. DSCH also features the symbols, models and assembly support for 8051 and 16F84 controllers. Designers can create logic circuits for interfacing by means of these controllers and verify software programs using DSCH.

A) Execution of the Clocked Pair Shared Flip Flop

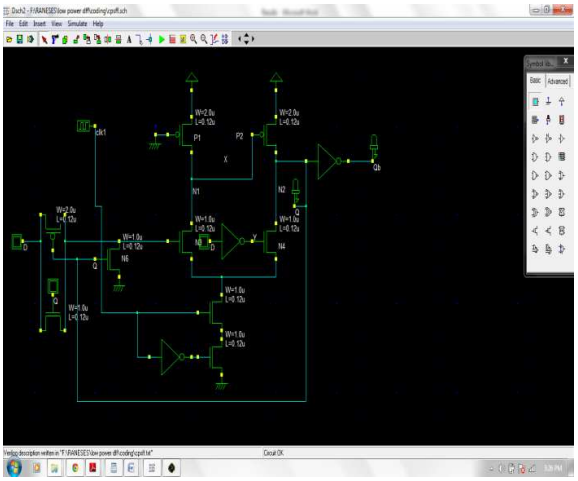


Fig.8. Execution of the Clocked Pair Shared Flip Flop

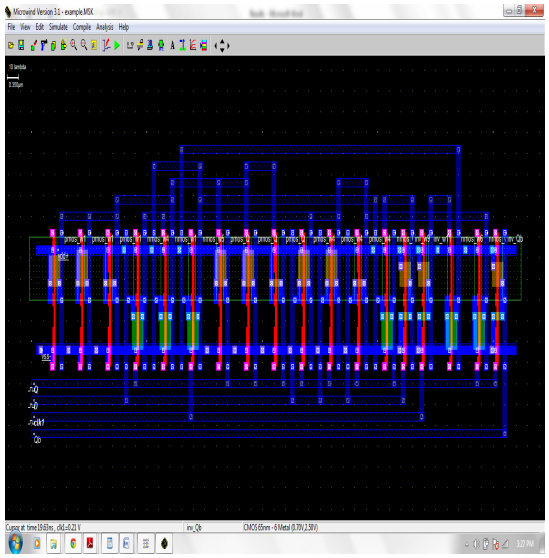
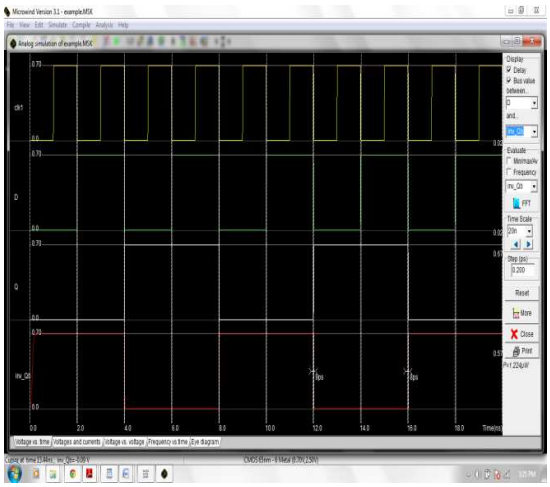


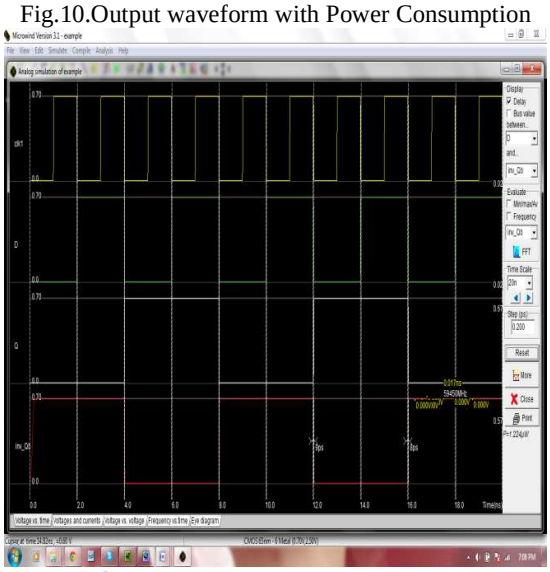
Fig.9.Layout in Microwind



Power = 1.224µw

Fig.10.Output waveform with Power Consumption



Delay=0.017ns, Frequency=59450MHZ

Table II

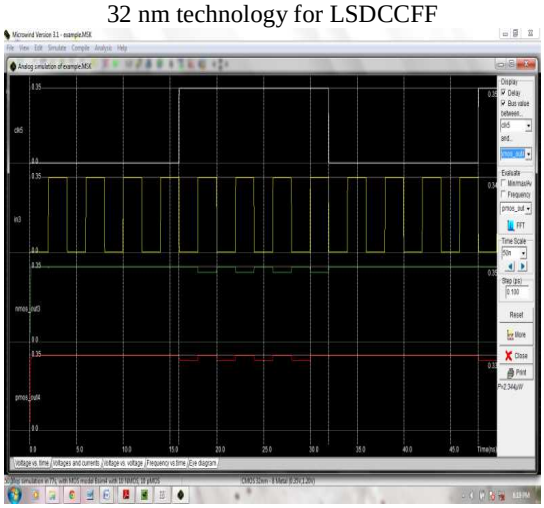
Comparing Flip-Flop in terms of Power, Delay and Frequency

| Flip Flops | Power(µw) | Delay (ns) | Frequency (MHZ) |
|---|---|---|---|
| CDMFF | 56.377 | 3.871 | 258 |
| LSDCCFF | 33.821 | 0.084 | 59450 |
| CPSFF | 1.224 | 0.017 | 59450 |

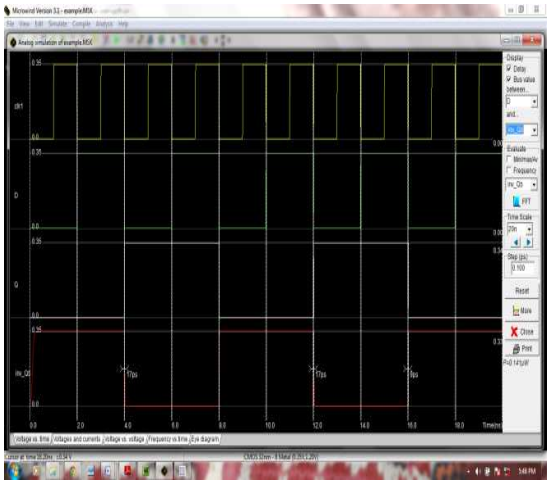
B) NANOMETER TECHNOLOGY COMPARISON OF LSDCCFF AND CPSFF

32 nm technology for LSDCCFF



Power=2.344µw

32 nm technology for CPSFF



Power=0.14u=µw

Table III
Comparison of Nanometer Technology output

| NM technology | LSDCCFF | CPSF (µw) |
|---|---|---|
| 32 | 2.344µw | 0.14 |
| 45 | 4.552µw | 0.221 |
| 65 | 33.821µw | 1.22 |
| 90 | 0.190mw | 8.297 |

## VI. CONCLUSION

In this paper, the arrangements of design techniques for low power clocking system are reviewed. One efficient method, reducing capacity of the clock load by minimizing amount of clocked transistor, is elaborated. Following the approach, one novel CPSFF is proposed, which reduces local clock transistor number by about

40%. In view of power consumption of clock driver, the most recent CPSFF outperforms prior arts in flip-flop design as a result of about 24%.

## REFERENCES


[1] Seyed E. Esmaeili, Asim J. Al-Kahlili, and Glenn E R. Cowan," Low-Swing Differential Conditional Capturing Flip-Flop for LC Resonant Clock Distribution Networks" IEEE Transactions on Very Large Scale Integration (VLSI) Systems, VOL. 20, NO. 8, AUGUST 2012.

[2] S. E. Esmaeili, A. J. Al-Khalili, and G. E. R. Cowan, "Estimating required driver strength in the resonant clock generator," in Proc. IEEEAsia Pacific Conf. Circuits Syst., 2010, pp. 927–930.

[3] S. E. Esmaeili, A. J. Al-Khalili, and G. E. R. Cowan, "Dual-edge triggered sense amplifier flip-flop for resonant clock distribution networks," IET Comput. Digit. Tech., vol. 4, no. 6, pp. 499–514, Nov.2010.

[4] V. F. Pavlidis, I. Savidis, and E. G. Friedman, "Clock distribution networks in 3-D integrated systems," IEEE Trans. Very Large Scale Integr. (VLSI)Syst.,10.1109/TVLSI.2010.2073724

[5] H. Mahmoodi, V. Tirumalashetty, M. Cooke, and K. Roy, "Ultra low power clocking scheme using energy recovery and clock gating," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 17, no. 1, pp. 33–44,Jan. 2009.

[6] Z. Xu and K. L. Shepard, "Design and analysis of actively-deskewed resonant clock network," IEEE J. Solid-State Circuits, vol. 44, no. 2,pp. 558–568, Feb. 2009.

[7] P. Zhao, J. McNeely, P. Golconda, M. A. Bayoumi, W. D. Kuang, and B. Barcenas,"Low power clock branch sharing double-edge triggered flip-flop," IEEE Trans. VeryLarge Scale Integr. (VLSI) Syst., vol. 15,no. 3, pp. 338–345, Mar. 2007.

[8] C. K. Teh, M. Hamada, T. Fujita, H. Hara, N. Ikumi, and Y. Oowaki,"Conditional data mapping flip-flops for low-power and high-performance systems," IEEE Trans. Very Large Scale Integr. (VLSI) Syst.,vol. 14, no. 12, pp. 1379–1383, Dec. 2006.

[9] F. H. A. Asgari and M. Sachdev, "A low-power reduced swing global clocking methodology," IEEE Trans. Very Large Scale Integr. (VLSI)Syst., vol. 12, no. 5, pp. 538–545, May 2004.

[10] P. Zhao, T. Darwish, and M. Bayoumi, "High-performance and lowpower conditional discharge flip-flop," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 12, no. 5,pp. 477–484, May 2004.

[11] A. J. Drake, K. J. Nowka, T. Y. Nguyen, J. L. Burns, and R. B. Brown,"Resonant clocking using distributed parasitic capacitance," IEEE J.Solid-State Circuits, vol. 39, no. 9, pp. 1520–1528, Sep. 2004.

[12] C. Kim and S. M. Kang, "A low-swing clock double-edge triggered flip-flop," in Proc. Symp. VLSI Circuits, 2001, pp. 183–186.

[13] J. Tschanz, S. Narendra, Z. P. Chen, S. Borkar,M. Sachdev, and V. De,"Comparativedelay and energy of single edge-triggered & dual edge triggered pulsed flip-flops forhigh-performance microprocessors," in Proc. ISPLED, Huntington Beach, CA, Aug.2001, pp. 207–212.

[14] B. Kong, S. Kim, and Y. Jun, "Conditional-capture flip-flop for statistical power reduction," IEEE J. Solid-State Circuits, vol. 36, no. 8, pp. 1263–1271, Aug. 2001.

[15] N.Nedovic, M.Aleksic, V.G. Oklobdzijia, "Conditional Precharge Techniques for Power-Efficient Dual-Edge Clocking" Int. Symp. Low-Power Electronics, Design, Monterey, CA, pp.56-59, Aug.2002.

[16] H. Kawaguchi and T. Sakurai, "A reduced clock-swing flip-flop (RCSFF) for 63%power reduction," IEEE J. Solid-State Circuits, vol.33, no. 5, pp. 807–811, May 1998