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RESEARCH ARTICLE

Design and Analysis of Register Element for Low Power Clocking System

Nagarajan.P[1], Dr.Saravanan.R[2]
[1]Assistant Professor, Department of ECE, PSNA College of Engg and Tech, Dindigul, India
[2]Professor, Department of CSE, PSNA College of Engg and Tech, Dindigul, India

[1]nagarajan.pandiyan@gmail.com; [2]hodcse@psnacet.edu.in

Abstract— The register element (flip-flop) is a basic building block to design any clocking system, which consists of the clock distribution tree and flip-flops. A large portion of the on chip power is consumed by the clocking system the total power consumption of the clocking system depends on both clocking distribution tree and also the register elements (flip-flops). The power consumption of register element is higher than that of the clocking distribution tree the objective is to reduce the power consumption by the register elements (flip-flop). A method of Conditional data mapping Flip Flop (CDMFF) was proposed earlier. The drawbacks of CDMFF are, it uses more number of transistors and it has a floating node on its critical path. Additionally it cannot be used in noise intensive environment. For that a method called Clocked Pair Shared Implicit pulsed Flip Flop (CPSFF) is proposed. In this method the number of transistors is reduced by sharing the clocked pair transistors. The floating node problem is also avoided by using precharge transistors. The design can be implemented in DSCH and MICROWIND 3.1 CMOS Layout tool. The performance is analyzed in views of number of transistors (N), Area (A), power (P), delay (D-Q), power delay product (PDP). Analysis of the performance parameters shows that performance of CPSFF is superior compared to the conventional Flip Flop. Overall power is reduced in CPSFF when compared to the previous method CDMFF. A 20% reduction of power can be achieved in Clocked Pair Shared Flip Flop (CPSFF). In addition due to the absence of floating node problem low swing voltage and dual edge clocking can be easily employed into the proposed register element (flip-flop) to construct clocking system.

Key Terms: - Flip flop; clocking system; register element; CMOS; delay; low-power

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