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RESEARCH ARTICLE

Implementation of High-Performance Image Scaling Processor using VLSI

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Abstract— In this paper, a less complexity, less memory requirement, and high performance algorithm is proposed for Very Large Scale Integration implementation of an image scaling processor. The anticipated image scaling algorithm consists of a clamp filter, spatial filter and a bilinear interpolation. The spatial and clamp filters are added as pre-filters for reducing the aliasing artifacts resulted by the bilinear interpolation. A T-model and inversed T-model convolution kernels are proposed to reduce the complexity of the design. Combined filter is replaced by a dynamic estimation unit to minimize the hardware cost. This architecture is targeted to produce 320MHz with 6.08-K gate counts. Compared with Previous methodologies, this work shows better performance with respect to cost and less complexity.

Key Terms: - Clamp filter; Image zooming; Dynamic estimation unit; Bilinear; Spatial filter; VLSI

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