



**RESEARCH ARTICLE**

# Implementation of Cryptographic Algorithm on FPGA

Prof. S. Venkateswarlu<sup>1</sup>, Deepa G.M<sup>2</sup>, G. Sriteja<sup>3</sup>

<sup>1</sup>Department of Computer Science, K L University, Vaddeswaram, Andhra Pradesh, India

<sup>2</sup>Department of Computer Science, K L University, Vaddeswaram, Andhra Pradesh, India

<sup>3</sup>Department of Computer Science, K L University, Vaddeswaram, Andhra Pradesh, India

---

***Abstract— Advanced Encryption Standard (AES), a Federal Information Processing Standard (FIPS), is an approved cryptographic algorithm that is used to protect electronic data. The AES can be programmed in software or built with hardware. The paper presents a hardware implementation of the AES algorithm on FPGA. The algorithm was implemented in FPGA using Spartan 3E starter kit and Xilinx ISE development suite. The purpose of this attempt was to test the correctness of the implemented algorithm and to gain experience in optimization of algorithm structure for the embedded implementation in the target application.***

***Key Terms: - AES algorithm; hardware implementation; FPGA***

---

Full Text: <http://www.ijcsmc.com/docs/papers/April2013/V2I42013108.pdf>