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RESEARCH ARTICLE

Hardware-Optimized Lattice Reduction Algorithm for WiMax/LTE MIMO Detection using VLSI

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Abstract— This paper presents the first ASIC implementation of an LR algorithm which achieves ML diversity. The VLSI implementation is based on a novel hardware-optimized LLL algorithm that has 70% lower complexity than the traditional complex LLL algorithm. This reduction is achieved by replacing all the computationally intensive CLLL operations (multiplication, division and square root) with low-complexity additions and comparisons. The VLSI implementation uses a pipelined architecture that produces an LR-reduced matrix every 40 cycles, which is a 60% reduction compared to current implementations. The proposed design was synthesized in both 130µm and 65nm CMOS resulting in clock speeds of 332MHz and 833MHz, respectively. The 65nm result is a 4X improvement over the fastest LR implementation to date. The proposed LR implementation is able to sustain a throughput of 2Gbps, thus achieving the high data rates required by future standards such as IEEE 802.16m (WiMAX) and LTE-Advanced.

Key Terms: - WiMax; MIMO; Lattice; LTE

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