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RESEARCH ARTICLE

Design of Low Power Dual Trigger Sequential Circuit

R. Balakumaresan[1], A. Selvapandian[2], S. Krishnakumar[3]

[1]Assistant Professor, Department of Electronics and Communication, PSNACET Dindigul, Tamilnadu, India
[2]Assistant Professor, Department of Electronics and Communication, PSNACET Dindigul, Tamilnadu, India
[3]Assistant Professor, Department of Electronics and Communication, TKSCTE, Dindigul, Tamilnadu, India

[1] rbalakumaresan@gmail.com; [2] selva6040@gmail.com; [3] krishnakumar.ksl@gmail.com

Abstract— A large portion of the on chip power is consumed by the clock system which is made of the clock distribution network and flip-flops. So the objective is to reduce the power consumption. Most of the on chip power is consumed by the clock system which is made of the clock distribution network and flip-flops. The "Conditional Data Mapping Flip Flop" (CDMFF) and "Clocked Pair Shared Implicit Pulsed Flip Flop" (CPSFF) are triggered using single edge of clock. In CPSFF, reducing capacity of the clock load by minimizing number of clocked transistor was elaborated. The drawbacks of single edge clocking system are high transistor count and floating node problem in critical path. Moreover it cannot be used in noise intensive environment. The CDMFF and CPSFF are triggered using single edge clocking system. Here, the design of a Dual triggered CMOS circuit is proposed. The objective is to reduce the number of clocked transistors and switching activities, thereby reducing the power dissipation. The proposed design is implemented in Microwind 3.1 and simulated using DSCH. The frequency of the Dual triggered CMOS circuit is only half of the clock frequency of the single edge triggered CMOS circuit. Simulation analysis shows that the Dual triggered CMOS circuit reduces switching activities by about 40%, thus reducing dynamic power dissipation. Hence it is suitable for using in high performance and low power environments.

Key Terms: - CDMFF; CPSFF

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