RESEARCH ARTICLE

Performance Analysis of Sequential Element for Low Power Clocking System

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Abstract— The sequential element (flip-flop) is a basic building block to design any clocking system, which consists of the clock distribution tree and flip-flops. A large portion of the on chip power is consumed by the clocking system the total power consumption of the clocking system depends on both clocking distribution tree and also the register elements (flip-flops). The power consumption of register element is higher than that of the clocking distribution tree the objective is to reduce the power consumption by the register elements (flip-flop). A method of Conditional data mapping Flip Flop (CDMFF) was proposed earlier. The drawbacks of CDMFF are, it uses more number of transistors and it has a floating node on its critical path. Additionally it cannot be used in noise intensive environment. For that a method called Clocked Pair Shared Implicit pulsed Flip Flop (CPSFF) is proposed. In this method the number of transistors is reduced by sharing the clocked pair transistors. The floating node problem is also avoided by using precharge transistors. The design can be implemented in DSCH and MICROWIND 3.1 CMOS Layout tool. The performance is analyzed in views of number of transistors (N), Area (A), power (P), delay (D-Q), power delay product (PDP). Analysis of the performance parameters shows that performance of CPSFF is superior compared to the conventional Flip Flop. Overall power is reduced in CPSFF when compared to the previous method CDMFF. A 20% reduction of power can be achieved in Clocked Pair Shared Flip Flop (CPSFF). In addition due to the absence of floating node problem low swing voltage and dual edge clocking can be easily employed into the proposed register element (flip-flop) to construct clocking system.

Key Terms: - Flip flop; clocking system; register element; CMOS; delay; low power

INTRODUCTION

The system on chip design is integrating hundreds of millions of transistors on one chip, whereas packaging and cooling only have a restricted ability to eradicate the excess heat. All of these results in power utilization being the tailback in achieving

high performance. The clock system which consists of clock distribution tree and the register elements (Flip Flops and Latches), is one of the most power consuming components in a VLSI system. It accounts for 20% to 40% of the total power dissipation of a system.

As a result minimizing the power consumed by register element will have a deep impact on the total power consumed. A large portion of the on chip power is utilized by the clock drives. Carefulness must be paid to reduce the clock load when construct a clocking system.

Many current microprocessors selectively use master-slave and pulse triggered Flip Flops. Traditional master-slave single edge Flip Flops for example transmission gated Flip Flops, are constructed by 2 stages, one master and another slave. All of these Flip flops are characterized by hard edge properties such as positive setup time causing huge D to Q delay.

On the other hand, pulse triggered Flip Flops diminish the two stages into one stage and are characterized by the soft edge property. 95% of all static timing latching on the Itanium processor is pulsed clocking. Pulse triggered Flip Flops could be classified into two types, implicit pulsed and explicit pulsed, for implicit pulse triggered data close to output Flip Flops (IP-DCO) and explicit pulse triggered data close to output Flip Flops (EP-DCO).

METHODOLOGIES FOR LOW POWER DESIGN OF REGISTER ELEMENT

Power consumption is determined by several factors including frequency f, supply voltage V, data switching activity $\square$, capacitance C, leakage current, and short circuit current.

$P = P_{Dynamic} + P_{short\ circuit} + P_{leakage}$ (1)

In the above equation, dynamic power $P_{dynamic}$ is also called

the switching power $P = \square CV^2 f$ (2)

$P_{short\ circuit}$ is the short circuit power which is caused by the finite rise and fall time of input signals, resulting in both the pull up network and pull down network to be ON for a short while.

$P_{short\ circuit} = I_{short\ circuit} \cdot V_{dd}$ (3)

$P_{leakage}$ is the leakage power. With supply voltage scaling down, the threshold voltage also decreases to maintain performance. However, this leads to the exponential growth of the subthreshold leakage current. Subthreshold leakage is the dominant leakage now.

$P_{leakage} = I_{leakage} \cdot V_d$ (4)

A. Dual Edge clocking

Using half frequency on the clock distribution network will save approximately half of the power consumption on the clock distribution network. However the flip-flop must be able to be double clock edge triggered. For example, the clock branch shared implicit pulsed flip-flop (CBS-IP DETFF), is a dual edge triggered flip-flop. Dual clock edge triggering method reduces the power by decreasing frequency f in (2).

B. Low Swing Voltage on Clock Distribution Tree

Using a low swing voltage on the clock distribution network can reduce the clocking power consumption since power is a quadratic function of voltage. To use low swing clock distribution, the flip-flop should be a low swing flip- flop. For example, low swing double-edge flip-flop (LSDFF) is a low swing flip-flop. In addition, the level converter flip-flop is a natural candidate to be used in low swing environment too. For example, CD- LCFF-ip, could be used as a low swing flip-flop since incoming signals only drive

nMOS transistors. The low swing method reduces the power consumption by decreasing voltage in (2).

C. Dual Threshold Voltage/MTCMOS

Using Dual Vt/MTCMOS to reduce the leakage power in standby mode. With shrinking feature size, the leakage current increases rapidly, the MTMOS technique as well as transistor stacking, dynamic body biasing, and supply voltage ramping could be used to reduce leakage standby power consumption .

Split path can reduce the short current power, since pMOS and nMOS are driven by separate signals.

D. Reducing Capacity of Clocked Transistors

80% of no clocked nodes have switching activity less than 0.1. This means reducing power of clocked nodes is important since clocked node has 100% activity. One effective way of low power design for clocking system is to reduce clock capacity load by minimizing number of clocked transistor. Any local clock load reduction will also decrease the global power consumption.

E. Reduction of Transient Activity

There are two ways to reduce the switching activity: conditional operation (eliminate redundant data switching conditional discharge flip-flop (CDFF), conditional capture flip-flop (CCFF)) or clock gating. The conditional operation technique is needed to control the redundant switching. In CDFF, a feedback transistor is inserted on the discharging path of 1st stage which will turn off the discharging path when D keeps 1. Internal node will not be kept discharging at every clock cycle.

F. Clock Gating

When a certain block is idle, we can disable the clock signal to that block to save power. Both conditional operation and clock gating methods reduce power by decreasing switching activity.

DESIGN OF CDMFF (CONDITIONAL DATA MAPPING FLIP FLOP)

A large portion of the on-chip power is consumed by the clock drivers. It is desirable to have less clocked load in the system. CDFF and CCFF both have many clocked transistors. For example, CCFF used 14 clocked transistors, and CDFF used 15 clocked loads. In contrast, conditional data mapping flip-flop (CDMFF, Fig1) used only seven clocked transistors, resulting in about 50% reduction in the number of clocked transistors, hence CDMFF used less power than CCFF and CDFF. (Note that CDFF used double edge clocking. This shows the effectiveness of reducing clocked loads numbers to achieve low power. Since CDMFF outperforms CCFF and CDFF in vision of power consumption.
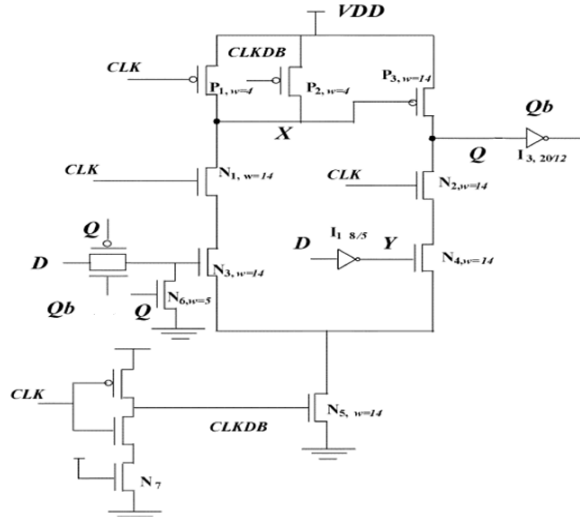
Fig. 1. Conditional Data Mapping Flip Flop (CDMFF)

However, there is redundant clocking capacitance in CDMFF. When data remains LOW or HIGH, the precharging transistors, P1 and P2, keep switching without useful computation, resulting in redundant clocking. Clearly, it is necessary to reduce redundant power consumption here. Further, CDMFF has a floating node on critical path because its first stage is dynamic. When clock signal CLK changes from LOW to HIGH, CLKDB will stay HIGH for a short while which produces an implicit pulse window for evaluation. During that window, both P1, P2 are off. In addition, if D transits from LOW to HIGH, the pull down network will be disconnected by N3 using data mapping scheme (N6 turns off N3); If D is LOW, the pull down network is disconnected from GND too. Hence internal node X is not connected with supply Vdd or GND.

With feature size shrinking, dynamic node is more prone to noise intermission because of the undriven dynamic node. If a close by noise discharges the node X, pMOS transistor P3 will be partially on, and a glitch will appear on output node Q. In a nanoscale circuit, a glitch consumes power and also propagates to the next stage which results the system more weak to noise. Hence, CDMFF could not be used in noise intensive environment. Unlike CDMFF, other dynamic flip-flops employ structure to prevent the floating point. Finally it is hard to apply the low power methods to CDMFF. For example, the clock structure with precharging transistors P1, P2 in CDMFF makes it difficult to apply double edge triggering. Nor can CDMFF be used in a low swing clock environment. (Note that the incoming low swing clock signal cannot drive pMOS, P1 and P2, in high voltage block (VDDH), because the pMOS transistors will not turn off by a low swing voltage, resulting in short circuit power dissipation).

DESIGN OF CPSFF (CLOCKED PAIR SHARED FLIP-FLOP BY REDUCING CLOCKED LOADS)
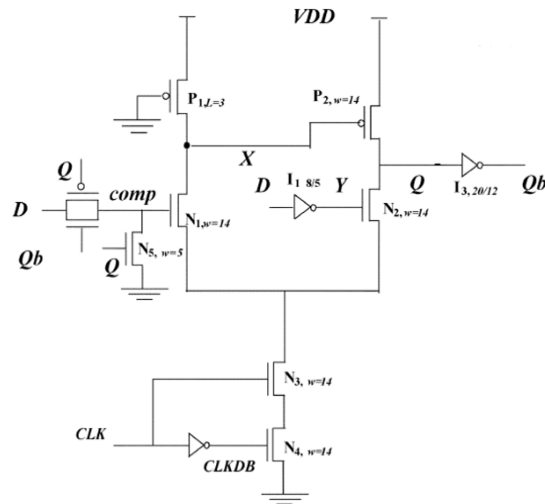

Fig. 2. Clocked Pair Shared Flip Flop (CPSFF)

CDFF and CCFF use many clocked transistors. CDMFF reduces the number of clocked loads but it has redundant clocking as well as a floating node. To ensure efficient and robust implementation of low power register element, Clocked Pair Shared flip-flop (CPSFF, Fig2) is proposed. It uses less clocked transistors than CDMFF and to defeat the floating problem in CDMFF.

In the clocked-pair-shared flip-flop, clocked pair (N3, N4) is shared by first and second stage of the latching part. The pseudo nMOS transistor (i.e) pMOS, P1, is used to charge the internal node X rather than using the two clocked pre charging transistors (P1, P2) in CDMFF. Comparing with CDMFF, a total of three clocked loads are reduced, such that the clock load seen by the clock driver is minimized, resulting in an efficient design. Further the transistor N7 in the clocked inverter in CDMFF is rejected. CPSFF uses four clocked loads rather than seven clocked loads in CDMFF, resulting in just about 40% reduction in number of clocked loads.

Additionally the internal node X is connected to supply Vdd by a pseudo nMOS P1, so is not floating, and results improvement of noise robustness of node X. This mitigates the floating point problem in CDMFF. The pseudo nMOS P1 is a weak pMOS transistor. This scheme combines pseudo nMOS with a conditional mapping method where a feedback signals, comp, controls the transistor nMOS N1. When input D stays HIGH, Q=1, N5 is ON, N1 will shut off to avoid the redundant transient activity at node X as well as any short circuit current. Pmos P2 should pull Q high when D switches to 1. The second nMOS branch (N2) is in charge for pulling down the output of Q if D = LOW and Y=1when the clock pulse arrives. pMOS in I1 should turn on Nmos N2 when D=LOW. Although P1 is always ON, short circuit only occurs one time when D makes a transition of LOW->HIGH, and the discharge path is disconnected after two gates delay by comp (turning off N1). After that, if D remains at HIGH, the discharge path is already disconnected by N1; there would be no short circuit. The clocked-pseudo-nMOS scheme is different from the general idea of conventional pseudo-nMOS logic in that we use clocked transistors in the pull down branch. P1, N1, N3, and N4 should be properly scaled to guarantee a correct noise margin. Several low power methodologies can be easily included into the new register element. Unlike CDMFF, low swing clock voltage method is possible for

CPSFF since arriving low voltage clock does not drive pMOS transistors. Low swing voltage clock signals could be connected to the nMOS transistors N3 and N4, respectively. Additionally, it is easy to construct dual edge triggering flip-flop based on the simple clocking construction in CPSFF. Further the incoming clock and data signals only drive nMOS transistors. So CPSFF could be used as a level converter flip-flop automatically.

SIMULATION RESULTS

The simulation results were obtained from DSCH & MICROWIND3.1 simulations in 0.12□m CMOS technology at room temperature. VDD is 1.2 V. A clock frequency of 250 MHz is used. Each design is simulated using the circuit at the layout level. Performance parameters such as Area, Power and Delay are obtained from layout simulation. Circuits were optimized for power delay product (PDP). Delay is data to output delay (D-to-Q delay) which is the sum of the setup time and the clock to the output delay.

CPSFF uses three less clocked loads, which leads to about 40% reduction in number of clocked loads. It achieves 25% less clock driving power consumption than CDMFF, which improves power efficiency significantly. This simulation set up of CPSFF in MICROWIND in fig.3 shows the reduction of Clocked loads. Internal node transient activities are avoided by means of pseudo nMOS precharge pMOS transistor P1 in schematic. The layout of CPSFF in fig.6 is generated in Microwind. Layout simulation gives the reduced area due to the reduced clock load. In view of the clocking load in the latch, the proposed clocked-pair shared flip-flop is more efficient than other designs like the CCFF, CDFF, CDMFF, etc. In terms of PDP, more than 7.6% improvement is achieved. Though there is contention between always on P1 and pull down path in the first stage, its negative PDP, more than effect on speed is alleviated by the reduction of capacitor load on internal node X, where two precharging clocked transistors are removed.

With feature size shrinking, the leakage current increases rapidly, and the MTMOS technique could be used to reduce the leakage power consumption. In addition, with technology scaling, process variation tolerant techniques like combinations of adaptive body bias and adaptive V_{dd} may be used to improve functionality and performance of the die. As CMOS technology continues scaling, integrated circuits are more susceptible to soft errors, soft-error-tolerant techniques could be used.
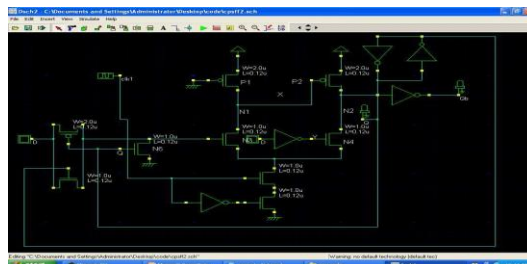

Fig. 3 Schematic of Clocked Pair Shared Implicit Pulsed Flip Flop
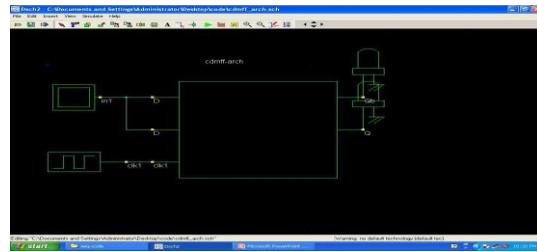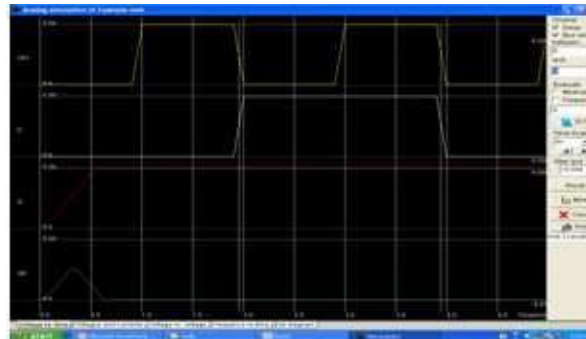
Fig.4 setup for testing the CPSFF
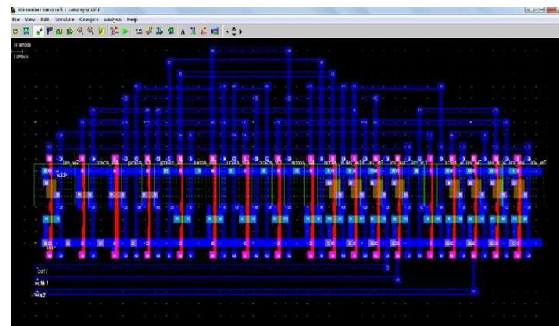

Fig. 5 Output waveform of CPSFF

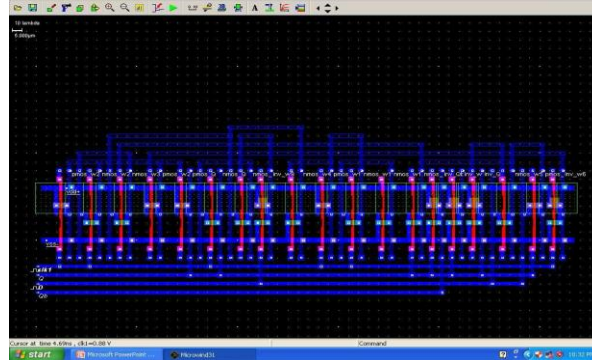Fig. 6 Layout Diagram of Clocked Pair Shared Flip Flop

Fig. 7 Layout Diagram of Conditional Data Mapping Flip Flop

TABLE I SIMULATION RESULTS OF CDMFF AND CPSFF

Register Element Name	No. of Transistors	No. of Clocked Transistors	Area (µm2)	Power (µW)	Delay (ps)	PDP (fJ)
CDMFF	22	7	1708	11.326	387	4.396
CPSFF	19	4	1040	6.935	392	2.724

CONCLUSION

In this paper, several design techniques for register elements are reviewed. One effective method, reducing capacity of the clocked load by minimizing number of clocked transistors, is elaborated. Following the approach, the register element CPSFF is proposed, which reduces local clock transistor number by about 40%. The performance analysis is carried out on the register element CPSFF. In view of power consumption, area and power delay product, the proposed CPSFF outperforms prior arts in register element design by about 24%. Furthermore, several low power techniques, like low swing and double edge triggering can be easily incorporated in to the proposed register element CPSFF.

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