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RESEARCH ARTICLE

Performance Analysis of Dual Tail Comparator for Low Power Applications

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Abstract— The dynamic regenerative comparators are used in analog to digital converters to reduce the power consumption, area and to increase the speed so it is necessary to design low power dynamic comparator for designing low power ADC. In this project, an analysis on the delay of the dynamic comparators is presented. From the analysis, an intuition about the main contributors to the comparator delay and the tradeoffs in dynamic comparator design are found. Based on that analysis, a new dynamic comparator is proposed, where the circuit of an existing double tail comparator is modified for low-power and fast operation even in small supply voltages. Without complicating the design and by adding few transistors, the positive feedback during the regeneration is strengthened, which results in remarkably reduced delay time. Post-layout simulation results in a 0.18-µm CMOS technology confirm the analysis results. It is shown that in the proposed dynamic comparator both the power consumption and delay time are significantly reduced.

Keywords— Double-tail comparator; dynamic clocked comparator; high-speed analog-to-digital converters (ADCs); low-power analog design

I. INTRODUCTION

A Comparator is one of the fundamental building blocks in most analog-to digital converters. Comparator is a circuit with two input terminals i.e. inverting and non inverting. a standard voltage known as reference voltage V_{ref} is connected to either inverting or non-inverting terminal. When it is connected to inverting terminal the input voltage Vin to compare is connected to non-inverting terminal or vice versa.

When the V_{ref} = 0 and it is connected to inverting terminal, then the circuit is called as inverting zero reference comparator. When it is connected to non inverting terminal, the circuit is called as non-inverting zero reference comparator. When the V_{ref} > 0 and it is connected to inverting terminal, the circuit is called as inverting non-zero reference comparator. When it is connected to non-inverting terminal, the circuit is called as non-inverting non-zero reference comparator.

Whatever may be the input condition, the output of the comparator can have only three possible values i.e. output voltage. $V_o = +V_{sat}$*(fully saturated positive voltage)* or output voltage will be as such that it will be $V_o = -V_{sat}$ *(fully saturated negative voltage).* Now consider inverting zero reference comparator. For this the value of $V_{ref} = 0$**.** The input voltage V_i is connected to non-inverting terminal. There are three possible conditions in this circuit, as follows.

When $V_i > V_{ref}$, $V_o = -V_{sat}$
When $V_i < V_{ref}$, $V_o = +V_{sat}$
When $V_i = V_{ref}$, $V_o = 0$

Now consider inverting non-zero reference comparator. Let Vref = 3V**.** The input voltage Vi is connected to inverting terminal. There are three possible conditions in this circuit, as follows.

When $V_i > V_{ref} = 3V$, $V_o = -V_{sat}$
When $V_i < V_{ref} = 3V$, $V_o = +V_{sat}$
When $V_i = V_{ref} = 3V$, $V_o = 0$

The above conditions occur because you are connecting higher i.e. positive voltage, which is greater than zero to inverting terminal. And the inverting terminal has the property to revert the polarity or sign of the voltage connected to it.

II. EXISTING SYSTEM

The main idea of the existing comparator is to increase Δ*V*fn/fp in order to increase the latch regeneration speed. For this purpose, two control transistors (*M*c1 and *M*c2) have been added to the first stage in parallel to *M*3/*M*4 transistors but in a cross-coupled manner.

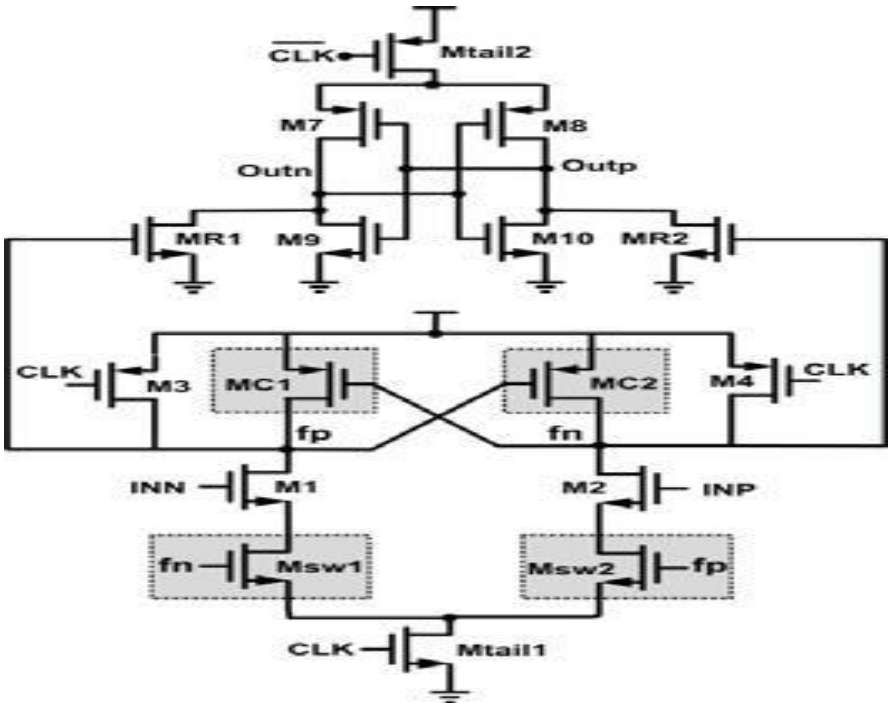

Fig.1 Existing Low power dual tail Comparator

The operation of the proposed comparator is as follows. During reset phase (CLK = 0, *M*tail1 and *M*tail2 are off, avoiding static power), *M*3 and *M*4 pulls both fn and fp nodes to *V*DD, hence transistor *M*c1 and *M*c2 are cut off. Intermediate stage transistors, *M*R1 and *M*R2, reset both latch outputs to ground. During decision-making phase (CLK = *V*DD, *M*tail1, and *M*tail2 are on), transistors *M*3 and *M*4 turn off. Furthermore, at the beginning of this phase, the controls transistors are still off since fn an fp are about *V*DD). Thus, fn an fp start

to drop with different rates according to the input voltages. Suppose *V*INP > *V*INN, thus fn drops faster than fp, (since *M*2 provides more current than M1).

As long as fn continues falling, the corresponding pMOS control transistor (*M*c1 in this case) starts to turn on, pulling fp node back to the *V*DD; so another control transistor (*M*c2) remains off, allowing fn to be discharged completely.

Despite the effectiveness of the above design, one of the points which should be considered is that in this circuit, when one of the control transistors (e.g., *M*c1) turns on, a current from *V*DD is drawn to the ground via input and tail transistor (e.g., *M*c1, *M*1, and *M*tail1), resulting in static power consumption. To overcome this issue, two nMOS switches are used below the input transistors [*M*sw1 and *M*sw2, as shown in fig.2] At the beginning of the decision making phase, due to the fact that both fn and fp nodes have been pre-charged to *V*DD (during the reset phase), both switches are closed and fn and fp start to drop with different discharging rates. As soon as the comparator detects that one of the fn/fp nodes is discharging faster, control transistors will act in a way to increase their voltage difference. Suppose that fp is pulling up to the *V*DD and fn should be discharged completely, hence the switch in the charging path of fp will be opened (in order to prevent any current drawn from *V*DD) but the other switch connected to fn will be closed to allow the complete discharge of fn node. Thus the power consumption is reduced in this design.

III. PROPOSED SYSTEM

One of the very important things that have to be noted is that though the above idea is very effective, there is still a serious problem in the design of the comparator. When transistor MC1 is ON, there is a static power consumption taking place, because the switch transistor Msw3 is still ON instead of going to OFF condition. To eradicate this problem two transistors Msw1 and Msw2 are added below the transistors Msw3 and Msw4. These transistors act as an additional switch, which goes OFF even before the switch transistors Msw3 and Msw4 goes to off state. This is because of the delay in the connecting wires. By this the power consumption in this comparator is improved. This proposed comparator consumes a power of 9.5µW. So the static power consumption is reduced which in turn reduces the leakage current.

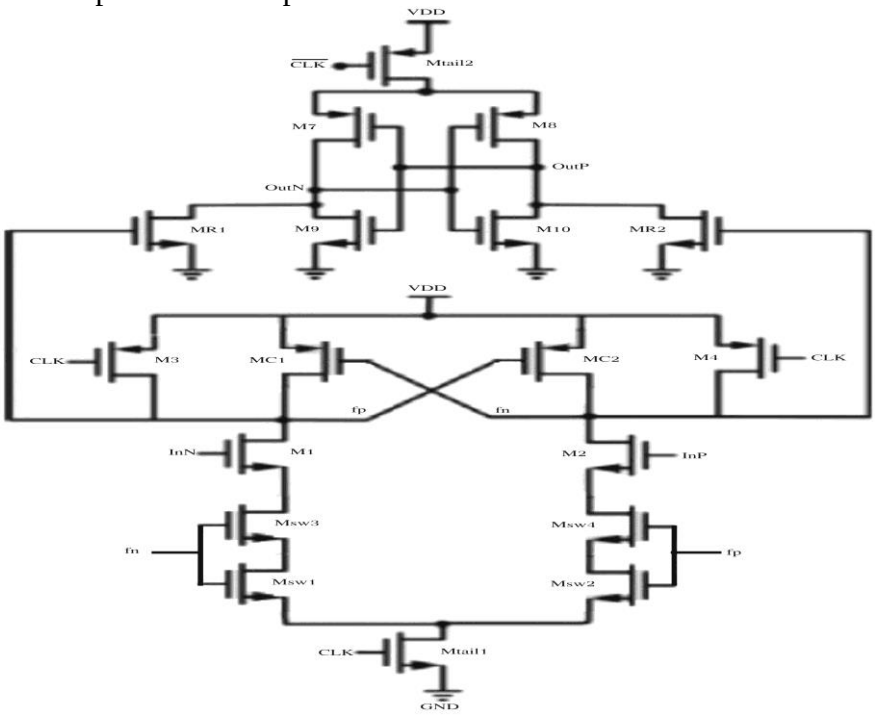

Fig.2 Proposed Low power Dual tail comparator

IV. SIMULATION SCREENSHOTS

In this paper a low power dual tail comparator was designed using tanner and it performance was compared with the existing dual tail comparator. The existing comparator designed using tanner is as shown below.

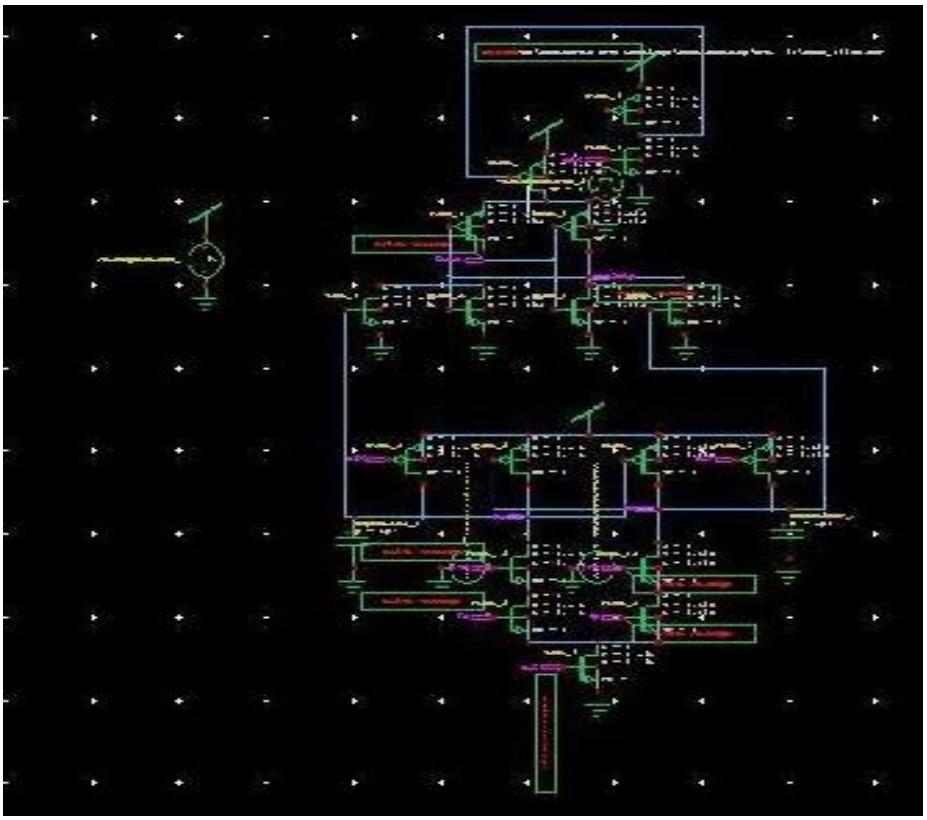

Fig.3 Existing comparator diagram

The power and delay report as well as the output waveform for the above circuit is as shown below.

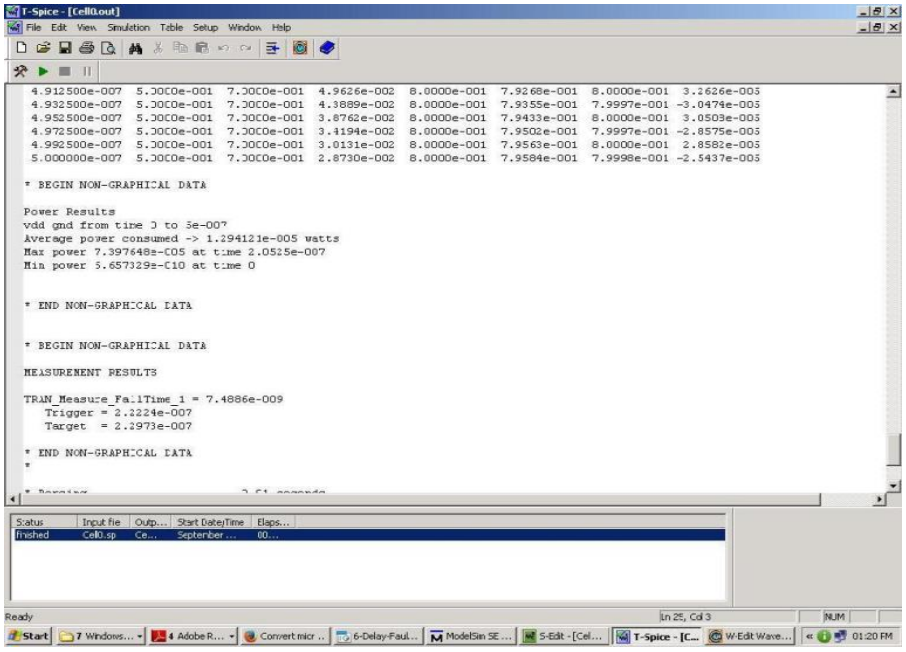

Fig.4 power and delay report

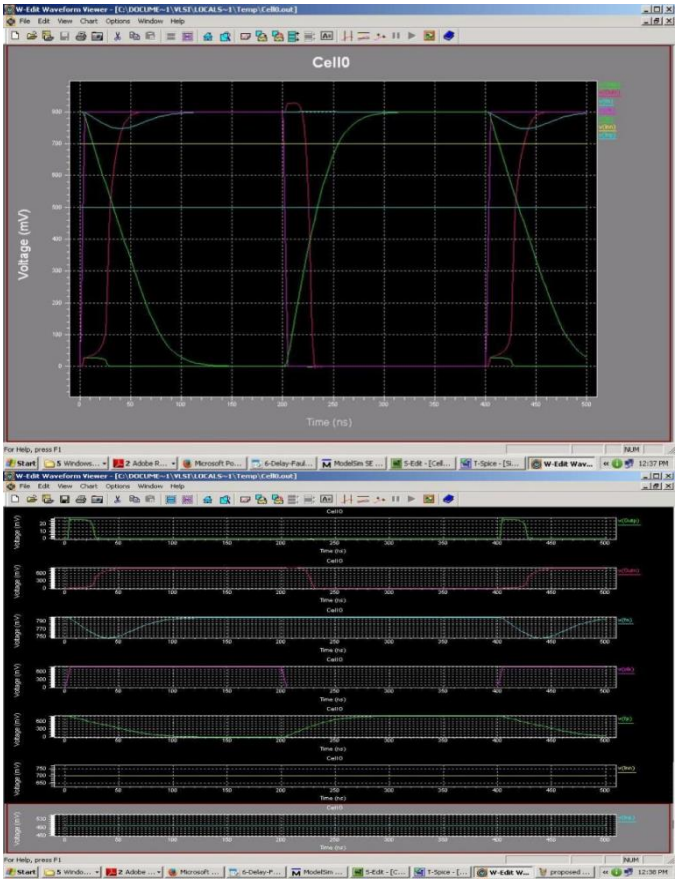

Fig.5 Output waveforms

The proposed dual tail converter designed using tanner is as shown below.

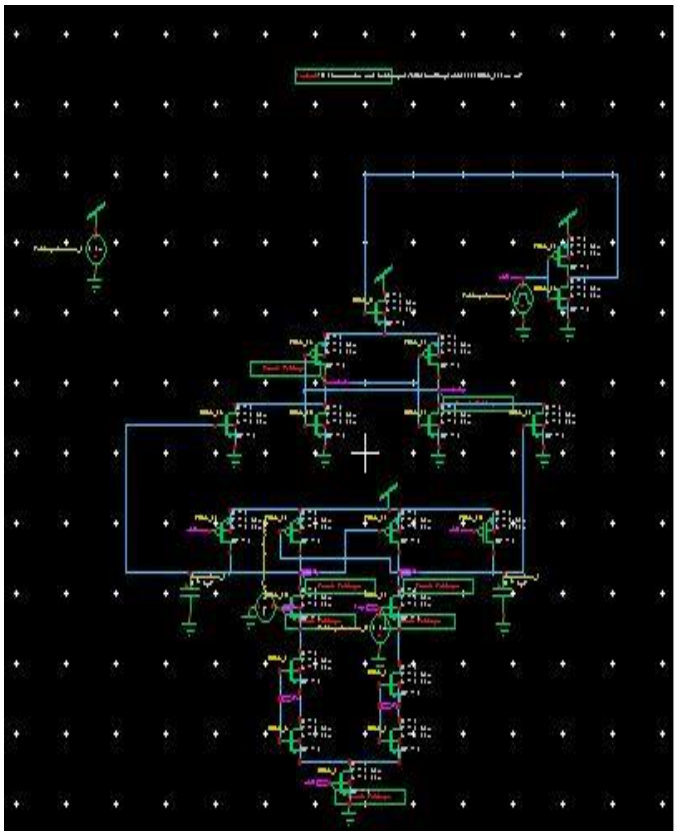

Fig.6 Proposed low power dual tail comparator diagram

The power and delay report as well as the output waveform for the above circuit is as shown below.

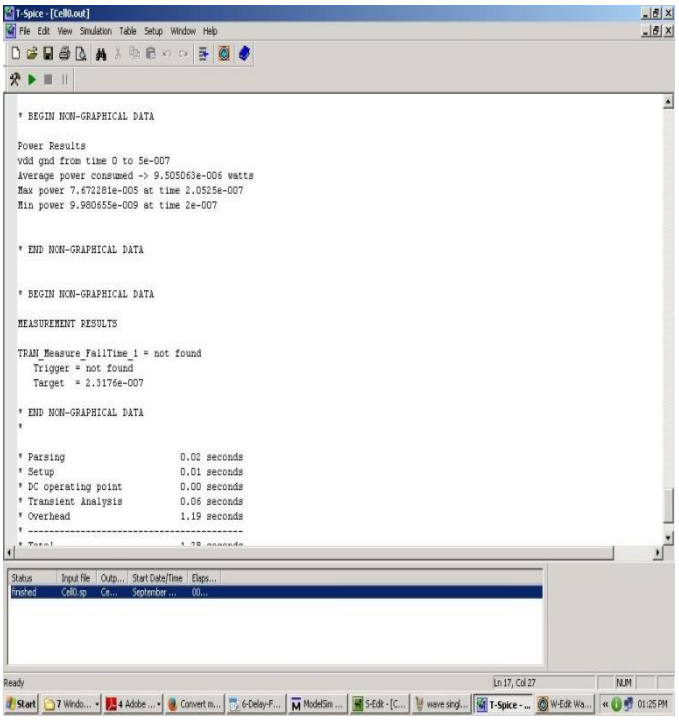

Fig.7 power and delay report

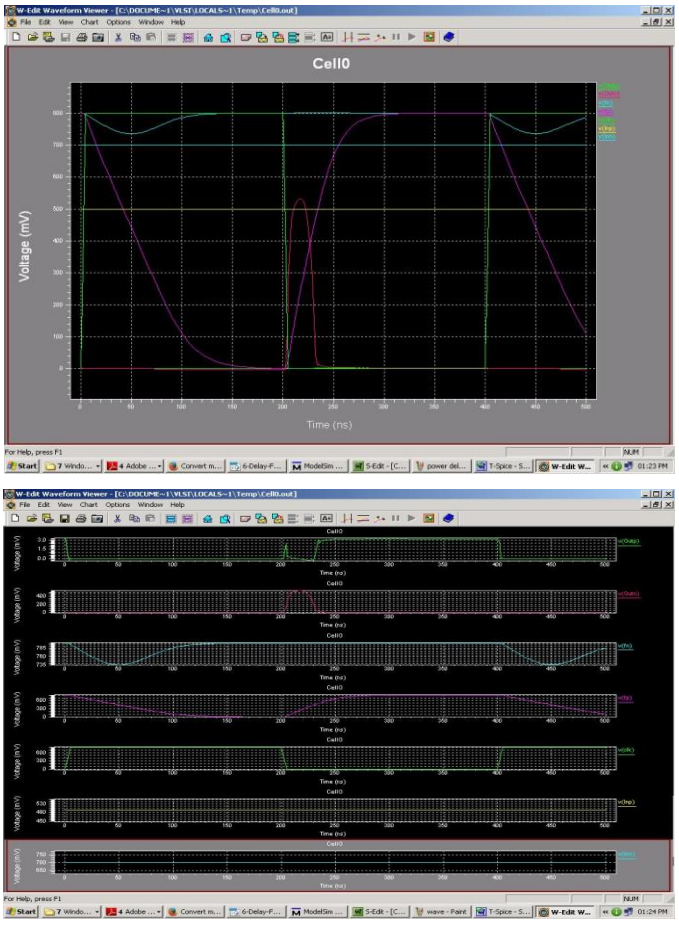

Fig.8 Output waveforms

The power and delay report obtained shows that the average power consumption of the existing comparator was 12µW. Then a low power dual tail comparator was designed by adding some additional transistors to the existing design and the design was simulated. The power and delay report obtained shows that the average power consumption of the designed comparator was 9.5 µW.

Process	Power
Existing	1.29*10-5 = 12µW
Proposed	0.95*10-5=9.5µW

V. CONCLUSIONS

In this paper a low power dual tail comparator is proposed and the proposed comparator circuit is simulated in tanner. In order to measure the efficiency of the proposed dual tail comparator the results are compared with the existing dual tail comparator. The results show that there is a reduction in power consumption of the proposed comparator. The future work involves using Low-Power High-Speed Flip Flops (LPHSFF) in the comparator design. This technique is based on CMOS multi-threshold voltage to reduce the number of transistors so that the area of the circuit can be minimized and also to save power dissipation thereby it increases the speed of operation of the circuits.

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