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RESEARCH ARTICLE

Low Power Flip-Flop Design for Low Swing LC Resonant Clock Distribution Networks

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Abstract— Low-power design is becoming a crucial design objective due to the growing demand on portable applications and the increasing difficulties in cooling and heat removal. The clock distribution network (CDN) delivers the clock signal which acts as a reference to all sequential elements in the synchronous system. The clock distribution network consumes a considerable amount of power in synchronous digital systems. Resonant clocking is an emerging promising technique to reduce the power of the clock network. The inductor used in resonant clocking enables the conversion of the electric energy stored on the clock capacitance to magnetic energy in the inductor and vice versa. This thesis describes a family of novel low-power flip-flops, which are suitable to work in low power low swing clock distribution networks. They achieve statistical power reduction by eliminating redundant transitions of internal nodes. The Conditional Capturing flip-flop is modified to operate with a low-swing sinusoidal clock. Low-swing resonant clocking achieved around 5.8% reduction in total power with 5.7% area overhead. Modeling the clock network with the existing Low Swing Differential Conditional Capturing Flip-Flop illustrates that low-swing clocking can achieve up to 58% reduction in the power consumption of the resonant clock. In order to achieve further power reduction, low swing sinusoidal clock with Clock Gating is introduced with modification in existing Flip Flops. Simulation results illustrate that by utilizing the proposed approach, more than 80% reduction in power consumption and approximately 85% reduction in noise level can be achieved.

Key Terms: - Clock; Flip-Flop; Low-Swing; Resonant Clock; Low Power; Clock Gated; Clock Distribution Network; Sinusoidal Clocking

I. INTRODUCTION

Microprocessor power consumption is increasing by approximately 20% per year. Approximately 30-50% of microprocessor power consumption is dissipated in the clock distribution network (CDN) which has the highest capacitance in the system and operates at high frequencies. The clock distribution network (CDN) in digital integrated circuits distributes the clock signal which acts as a timing reference controlling data flow within the system. CDN consumes a large amount of total power in synchronous systems. The CDN and latches dissipate around 70% of the IBM POWER4 1.3GHz microprocessor's power [2]. Latest developments in integrated circuit design specifically in 3-D integration where multi-plane synchronization is required, lead us to believe that the power consumption of the CDN will remain at these high levels [3].

CDN power dissipation can be expressed as

$$P = \alpha f C_L V_{dd} V_{SW} \quad (1)$$

where α is the switching activity, f is clock frequency, C_L is clock load Capacitance, Vdd is the supply voltage and V_{SW} is the clock voltage swing.An attractive approach to reduce power is to scale down the supply voltage which has a quadratic effect on power consumption.

However, scaling down the supply voltage would require decreasing the transistor threshold voltage level in order to maintain transistor driving capability. This leads to substantial increase in leakage power. In addition, decreasing the supply voltage would increase system susceptibility to variations. As a result, there is an increasing demand for power reduction schemes that do not require a reduction in the supply voltage.

Resonant clocking enables the generation of clock signals with reduced power consumption where low energy dissipation is achieved by recycling the energy stored on the clock capacitance. From the three resonant clocking techniques offered to date, namely: standing-wave, rotary traveling-wave, and LC resonant clocking; LC resonant clocking has proven to be the most convenient since it requires minimum change from conventional square-wave design and its practicality was verified on functional chips[12].

The traditional approach for LC resonant CDNs is to use the LC tank to drive the global clock distribution while the local square clock is being delivered through conventional buffers. However, around 66% of clock power is being dissipated in the last buffer stage driving the flip-flops [4], leading to minor power savings in LC globally-resonant locally-square CDNs. In order to achieve maximum power savings, the LC tank should drive the entire clock network (both global and local) without using intermediate buffers. Power reduction techniques for LC resonant CDNs in which the entire network including the flip-flops is being driven with a resonant (sinusoidal) clock signal will be the focus of this dissertation. Given that the bulk of the CDN capacitance is on its leaves, the largest power advantage will come by extending the LC resonance down to the flip-flops. This would require designing, modifying and understanding flip-flop performance with the sinusoidal clock signal generated in LC resonant networks.

C. Kim *et al.* [5] demonstrated that a low-swing square-wave clock double-edge triggered flip-flop has enabled 78% power savings in the CDN. Low-swing clocking would normally require two voltage levels, Vdd and Vdd_low. These voltage levels can be generated using one of two schemes: 1) dual-supply voltages and 2) regular power supply. The former achieves the reduced swing by using a reduced supply voltage usually generated on chip. The first scheme adds circuit and extra area complexity to the overall chip design and layout. However, it leads to a reduction in the number of clock network transistors which improves power savings [6]. The second scheme uses circuit methods to achieve low-swing. However, the design of low-swing buffers becomes challenging in the absence of a second power supply [6]. Several papers have proposed reduced swing buffers. Most of them utilize a pMOS for passing low logic level and an nMOS for passing high logic level. Such a technique results in poor rise and fall times making it impractical for high performance applications.

A similar approach to the one proposed in [4] is followed here in which the clock buffers are removed to allow the global and local clock energy to resonate between the inductor and entire clock capacitance including the receiving end flip-flops thus enabling maximum power savings. In addition, removing the clock buffers simplifies LC low-swing clocking since only reduced swing buffers are used at the flip-flop gate and not in intermediate levels within the clock tree [7].

II. SYSTEM OVERVIEW

CDNs in synchronous digital integrated circuits deliver the clock signal that controls the flow of data within the system. The input at each clock sink, i.e., flip-flop, is captured at the rising or falling clock edge (single-edge triggered flip-flops), or on both edges of the clock (dual-edge triggered flip-flops), or based on the voltage level of the clock (latches). The main objectives in the design of CDNs are to minimize skew, jitter, and power. Clock skew is defined as the difference in the arrival time of the clock edges at different locations in the CDN. Skew is mainly caused by variations between clock buffers, interconnect widths, and loading at different clock paths. Clock jitter is defined as the difference in the arrival time of the clock edge at the same location in the CDN. Jitter can make the clock period shorter or longer than nominal period. Jitter is mainly caused by temperature variation, power supply noise, and the phase-locked loop (PLL). 40% of the power in the 200 MHz 21064 Alph microprocessor is dissipated in the CDN.

A. Clock Distribution Network Structure

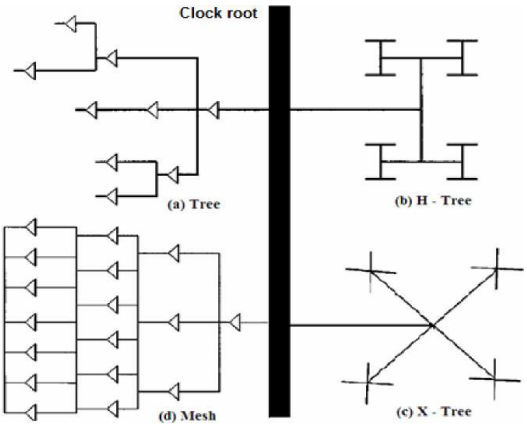

Figure 1 Common structure of clock distribution networks

Various clock distribution structures have been developed given that the routing area and complexity, speed and power dissipation of the system are all factors affected by the clock network design. Figure 1 illustrates common CDN structures. An asymmetric buffered tree structure is shown in Figure 1(a). In this structure, the wire as well as the buffer delay is balance in each path in order to achieve zero skew at the clock leaves. When the clock sinks are uniformly distributed, a symmetrical tree structure is used such as the H- and X- tree structures shown in Figure 1(b), (c). Although the balanced trees shown in the figure are not buffered, buffers are usually inserted to drive different sections of the tree. Properly matched buffers and interconnect delays as well as loading capacitances in clock trees can achieve under ideal conditions zero skew. However, in reality some skew will certainly be present due to variations in interconnect parameters as well as mismatches in clock buffers. Clock grid or mesh Figure 1(d) is another alternative to distribute the clock signal. The mesh actively reduces skew by connecting path resistances in parallel. In the mesh structure, the skew is independent of unbalanced distribution of loading. However, unlike clock trees, the mesh structure uses more wiring resources and consumes more power.

B. Resonant Clocking Techniques.

Resonant clocking reduces power dissipation in CDNs while enabling the generation of high frequency clock signals. There are three resonant clocking techniques offered to date. The first one is the standing wave oscillation which generates a clock signal with varying amplitude and constant phase. The second technique is the travelling rotary-wave oscillation which generates a clock signal with constant amplitude and varying phase making it suitable for non-zero clock skew systems. The third technique is the LC oscillation which generates a clock signal with constant amplitude and phase and requires minimum change from conventional clock design.

C. *LC Resonant Clocking.*

Figure 2(a) illustrates a simplified balanced clock tree structure for a conventional square-wave based CDN. Buffers are used to drive different sections in the tree. As shown in the figure, the clock signal propagating in the global tree to the lower branches which in turn feed the local clock and flip-flops is a square-wave clock signal. A globally-resonant locally-square CDN is shown in Figure 2(b). An inductor is connected at the center of the H-tree in order to generate a resonating clock signal at the fundamental frequency of the clock node.

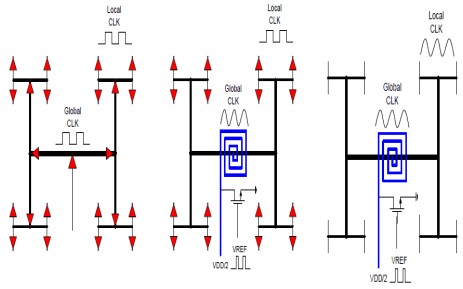

Figure 2 Simplified Square-wave, globally- and fully-resonant CDNs

Lower branches of the H-tree are driven by buffers which in turn convert the sinusoidal clock to square-wave signal feeding the flip- flops.. The buffers in globally-resonant locally-square CDN are removed in Figure 2(c) where the resonant clock signal is distributed all the way down to the flip-flop level. In resonant clocking, the largest power advantage is achieved by extending the resonance all the way down to the flip-flop level given that the bulk of the capacitance is in the leaves of the clock tree. In this approach, the clock buffers are removed to allow the clock energy to resonate between the inductor and the clock capacitance .Despite the promising power savings achieved in resonant CDNs, resonant clocking presents several design challenges because of the dependency of the clock rise time on its frequency and the susceptibility to process variation due to the long rise time of the clock, the need for different inductor values to generate different frequencies, the additional chip area occupied by the inductor.

By using logic gates (NAND/NOR), clock gating in conventional square-wave CDNs is achieved by using an ENABLE signal that controls the clock feeding a specific sector. However, this approach is not desirable in LC resonant CDNs since it would reduce the energy being recovered from the remaining capacitance of that sector. In [8], a clock gating scheme was proposed for LC resonant CDN by adding a NOR gate with an ENABLE signal at the clock input of every resonantly clocked flip-flop. Simulation results show that clock gating would reduce the power consumption of the flip-flop by more than 1000× in the idle mode compared to the power consumed without clock gating for 50% data switching activity. However, the extra routing resources and complexity of connecting the ENABLE signal to the input of each flip-flop as well as the power overhead associated with it was neglected**.**

D. *Sinusoidally clocked Flip-Flops.*

LC resonant clocking up to this date, is the most developed and practical resonant clocking technique. The clocking scheme adopted and assumed in this dissertation from here on is the fully-resonant LC scheme. The clock signal feeding the flip-flops is assumed to be purely sinusoidal clock since extending the resonance down to the flip-flop level results in most power savings. The long rise time of the sinusoidal clock signal compared to that of the square clock where the rise time is restricted to around 10-20% of the clock period affects the flip-flop speed, power, and susceptibility to variations.

III. **PREVIOUS WORKS**

A. Conditional Data Mapping Flip-Flop (CDMFF)

A large part of the on-chip power is consumed by the clock drivers. It is desirable to have less clocked load in the system. CDFF (Conditional Discharge Flip-Flop) and CCFF (Conditional Capture Flip-Flop) have many clocked transistors. For example, CCFF used 14 clocked transistors, and CDFF used 15 clocked transistors. In contrast, conditional data mapping flip-flop (CDMFF, Figure 3) used only seven clocked transistors, resulting in about 50% reduction in the number of clocked transistors, hence CDMFF has less power than CCFF and CDFF. CDFF used double edge clocking, for simplicity purpose, the power savings by double edge triggering on the clock distribution network is not discussed here. This shows the effectiveness of reducing clocked transistor numbers to achieve low power.

However, there is redundant clocking capacitance in CDMFF. When data remains 0 or 1, the pre-charging transistors, P1 and P2, keep switching without useful computation, resulting in redundant clocking. Clearly, it is necessary to reduce redundant power consumption here. Further, CDMFF has a floating node on critical path because its first stage is dynamic. When clock signal CLK transits from 0 to 1, CLKDB will stay 1 for a short while which produces an implicit pulse window for evaluation. During that window, both P1, P2 are off. In addition, if D transits from 0 to 1, the pull down network will be disconnected by N3 using data mapping scheme (N6 turns off N3); If D is 0, the pull down network is disconnected from GND too. Hence internal node X is not connected with Vdd or GND during most pulse windows, it is essentially floating periodically.

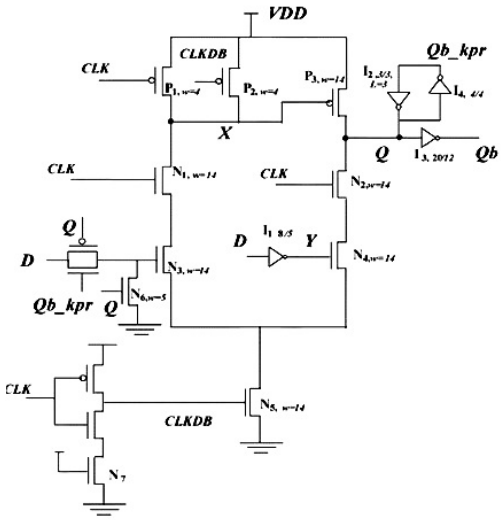

Figure 3 Conditional Data Mapping Flip-Flop

With feature size shrinking, dynamic node is more prone to noise interruption because of the non-driven dynamic node. If a nearby noise discharges the node X, pMOS transistor P3 will be partially on, and a glitch will appear on output node Q. In a nano scale circuit, a glitch not only consumes power but could propagate to the next stage which makes the system more vulnerable to noise. Hence, CDMFF could not be used in noise intensive environment. Unlike CDMFF, other dynamic flip-flops employ structure to prevent the floating point.

B. Low-Swing Differential Conditional Capturing Flip-Flop (LS-DCCFF)

Figure 4 shows LS-DCCFF. Conditional capturing is used to minimize flip-flop power at low data switching activities by eliminating redundant internal transitions. DCCFF operates in a pre-charge and evaluate fashion. Pull-up PMOS transistors are used for charging nodes SET and RESET. The effect of charge sharing can be reduced by ensuring a constant path to VDD. This is done by properly sizing the PMOS transistors. A short evaluation interval occurs after the rising edge of the clock when both the clock and inverted clock signals applied to transistors MN1/MN2 are above the threshold voltage level of the NMOS transistor. The DCCFF uses a NAND latch for storage. Using feedback from the output to control transistors MN3 and MN4 in the evaluation paths ensures conditional capturing. Therefore if the state of the input data is not changed, SET and RESET are not discharged.

As shown in Figure 4, reduced swing inverters are used at the node fed by the low-swing sinusoidal clock signal. This is done to reduce short circuit power by minimizing the interval at which both the PMOS and NMOS of the inverter turn on simultaneously. The load PMOS transistor in the reduced swing inverters is always in saturation since Vgs=Vds. It lowers the voltage at the source of the second PMOS in each inverter to approximately Vdd-|Vtp| thus turning it off when the low-swing sinusoidal clock signal reaches its peak voltage. The peak voltage for the low-swing clock was chosen to be equal to 0.65V since the threshold voltage of the PMOS transistor is approximately-0.34V.

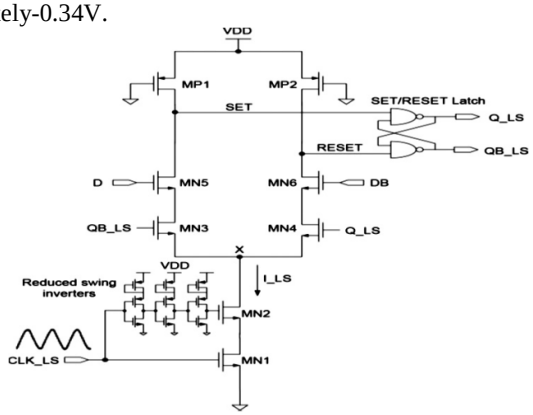

Figure 4 Low Swing Differential Conditional Capturing Flip Flop

C. Power

Following the approach proposed by the authors in [9] and [10], the power dissipation of the resonant clock network is given by the following equation

$$\text{Presonant\_clk} = \frac{Rclk}{2}\left(\pi f V_{peak}(C_{clk}+\alpha N C_{FF})\right)^2 \quad (3)$$

where *Rclk, Cclk* are the clock capacitance and resistance as seen by the driver, f and Vpeak are the frequency and peak voltage of the generated clock signal, C_{FF} is the loading capacitance of the flip-flop, N is the number of flip-flops, and α is the factor by which the loading capacitance of the flip-flop connected at clock leaves is reflected to the driver side. Equation (3) illustrates that generating a low-swing clock signal with Vpeak = 0.65Vdd results in around 58% power reduction in the clock network.

D. Modified Circuit for Full and Low swing Clocking.

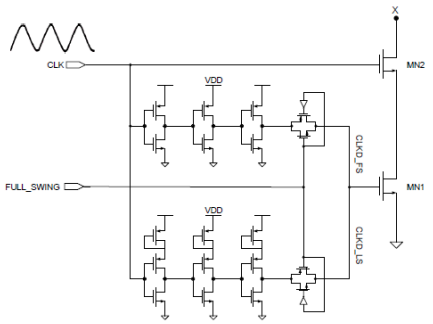

Figure 6 Modification to enable full- and low-swing flip-flop clocking

As illustrated in Figure 6, the LS-DCCFF presented in Figure 4 was modified at node X to allow the operation under full- and low-swing clocking. When signal FULL_SWING is high, full-swing clocking is enabled and the inverted clock output of the normal inverters CLKD_FS is feeding transistor MN1. Whereas Low-swing clocking is enabled when signal FULL_SWING is low and the output of the reduced voltage swing inverters CLKD_LS feeds transistor MN1.

IV. VARIOUS TECHNIQUES TO LOWER POWER CONSUMPTION

$$P = Pdynamic + Pshort\ circuit + Pleakage \quad (4)$$

In the above equation, dynamic power $P_{dynamic}$ is also called the switching power,

$$Pdynamic = \alpha CV2f. \quad (5)$$

$P_{short\ circuit}$ is the short circuit power which is caused by the finite rise and fall time of input signals, resulting in both the pull up network and pull down network to be ON for a short while.

$$Pshort\ circuit = I\ short\ circuit\ Vdd. \quad (6)$$

$P_{leakage}$ is the leakage power. With supply voltage scaling down, the threshold voltage also decreases to maintain performance. However, this leads to the exponential growth of the sub threshold leakage current. Sub threshold leakage is the dominant leakage now.

$$Pleakage = IleakageVdd \quad (7)$$

Based on these factors, there are various ways to lower the power consumption shown as follows.

1) *Double Edge Triggering:* Using half frequency on the clock distribution network will save approximately half of the power consumption on the clock distribution network. However the flip-flop must be able to be double clock edge triggered. Double clock edge triggering method reduces the power by decreasing frequency *f* in equation.

2) Using a low swing voltage on the clock distribution network can reduce the clocking power consumption since power is a quadratic function of voltage. To use low swing clock distribution, the flip-flop should be a low swing flip- flop. The low swing method reduces the power consumption by decreasing voltage in equation.

3) There are two ways to reduce the switching activity: conditional operation (eliminate redundant data switching: conditional discharge flip-flop (CDFF), conditional capture flip-flop (CCFF) or clock gating.

a) *Conditional Operation.*

For dynamic and semi dynamic flip-flop (SDFF), there are redundant switching activities in the internal node. When input stays at logic one, the internal node is kept charging and discharging without performing any useful

computation. The conditional operation technique is needed to control the redundant switching. For example, in CDFF, a feedback transistor is inserted on the discharging path of 1st stage which will turn off the discharging path when *D* keeps 1. Internal node will not be kept discharging at every clock cycle. In CCFF, it neither uses a clocked NOR gate to control an nMOS transistor in discharging path when *Q* keeps 1.The redundant switching activity is removed in both cases. This reduces the power consumption by decreasing data activity in the equation.

b) *Clock Gating.*

When a certain block is idle, we can disable the clock signal to that block to save power. Both conditional operation and clock gating methods reduce power by decreasing switching activity.

4) Using Dual Vt/MTCMOS to reduce the leakage power in standby mode. With shrinking feature size, the leakage current increases rapidly, the MTMOS technique as well as transistor stacking, dynamic body biasing, and supply voltage ramping could be used to reduce leakage standby power consumption.

5) *Reducing Short Current Power:* split path can reduce the short current power, since pMOS and nMOS are driven by separate signals.

6) *Reducing Capacity of Clock Load:* 80% of non-clocked nodes have switching activity less than 0.1. This means reducing power of clocked nodes is important since clocked node has 100% activity.

One effective way of low power design for clocking system is to reduce clock capacity load by minimizing number of clocked transistor. Any local clock load reduction will also decrease the global power consumption. This method reduces power by decreasing clock capacity in equation.

V. PROPOSED SYSTEM

LS-DCCFF works with low swing through the utilization of reduced swing inverters. There are four stacked transistors in the evaluation path, significant charge sharing may occur when three of them become ON simultaneously. This will cause significant current, and noise is also high. To ensure efficient and robust implementation of low power, low noise sequential element in CDN applications, we have modified the existing conditional capturing flip flop and named it as Low Power Low Swing Clock Gated Flip Flop (LPLSCGFF). To ensure efficient implementation and to overcome the problem associated with previous implemented design, the concept of sharing is used in this design. In this scheme, the two groups of clocked branches N3 and P3 shares the clock signal. The advantage of this sharing concept is reflected in reducing the number of clocked transistors required to implement the clocking system. Recall that clocked transistors have a 100% switching activity and consumes large amount of power. Reducing the number of clocked transistors is an efficient way to reduce the power.

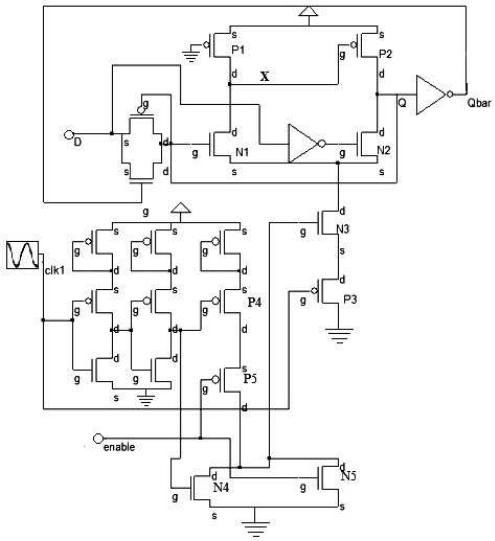

Figure 7 Low Power Low Swing Clock Gated Flip-Flop

In the Low Power Low Swing Clock Gated flip-flop, clocked pair (N3,P3) is shared by first and second stage. Sinusoidal low swing clock signal is level shifted by the low swing inverter comprising of 9 transistors. Clock gating is implemented with a NOR gate comprising two nMOS transistors and two pMOS transistors.

Flip Flop has an always on pMOS, P1, which is used to charge the internal node X rather than using the two clocked pre-charging transistors (P1, P2) as in CDMFF.

The internal node X is connected to Vdd by an always on P1, so X is not floating, resulting in enhancement of noise robustness of node X. This solves the floating point problem in CDMFF. The always ON P1 is a weak pMOS transistor (length = 3X). This scheme combines pseudo nMOS with a conditional mapping technique where a feedback signal, controls nMOS N1.

The clock generally has idle states during which it can be turned off else it would continue to run and consume the same amount of power as in the active state. We develop a clock gating technique for the oscillator to reduce the power consumed during the idle state. The proposed energy recovery clock generator with clock gating feature is shown in the Fig.8.It is a general set up and either NAND or NOR can be used for this purpose.

A NOR gate circuit which makes the output low when one or both the inputs are high. The clock gating circuit is connected with the clock pair stage. We can save power by disabling the clock network during the sleep mode as significant amount of power is consumed by the clock network. The input to the NOR gate is (a) a clock input and (b) an enable input. From the circuit given below the clock input is connected to the clock pair stage. When clock and enable signals are made high, which is connected to the clock pair stage makes the two transistors ON there by providing connection to ground.

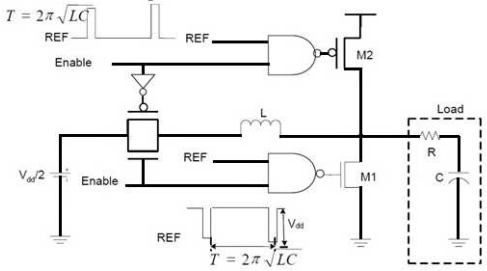

Figure 8 Energy Recovery Clock Generators with Clock Gating

The clock gating is implemented by replacing the inverters with the NAND gates that have the REF pulse and enable signal as their inputs. Moreover, a pass transistor switch is inserted in the half Vdd supply path to eliminate short circuit power in the clock gated mode when the pull down transistor is pulling the clock down to zero voltage. The pass transistor switch has to be a strong switch to reduce its associated loss of oscillator power efficiency. When the clock generator is active the enable signal is high and the switch is ON and when the clock generator is in an idle state the enable is low which would turn OFF the switch and the pull-up PMOS (M2) and turn ON the pull-down NMOS (M1).Hence, in the clock gated mode, the clock is gated to zero voltage and there is no switching happening at the gate of M1 and M2 transistors. This results in a substantial power saving in the oscillator.

Several low power techniques can be easily incorporated into the new flip-flop. The Dynamic power consumption in any CMOS circuit can be reduced by minimizing the switching activity, clock frequency, clock load capacitance, voltage swing and supply voltage. In the proposed flip flop conditional capturing technique is used to reduce the switching activity by eliminating redundant internal transitions. This is implemented by using a feedback from output to the input. As shown in Figure 7, reduced swing inverters are used to reduce the short circuit power. Clock gating is also implemented with the help of a NOR gate.

Unlike CDMFF, low swing is possible since incoming low voltage clock does not drive pMOS transistors. Low swing voltage clock signals could be connected to the transistors N3 and P3, respectively. In addition, it is easy to build double edge triggering flip-flop based on the simple clocking structure in proposed Flip-Flop. Further this could be used as a level converter flip-flop automatically, because incoming clock and data signals only drive nMOS transistors.

VI. SIMULATION AND MEASUREMENTS

Circuits are simulated using software packages DSCH, LT SPICE, Microwind, and Tanner (V13). Flip flops are tested by applying pulse input and verified its outputs. Verilog coding for the circuits are obtained from the simulation tool. Simulation results show that there is considerable reduction in power consumption and Noise in the proposed LPLSCGFF compared to the previous works.

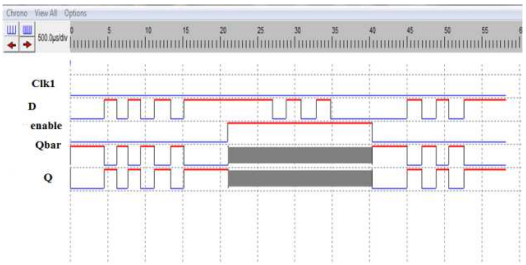

Figure 9 Timing Diagram for LPLSCGFF

VII. CONCLUSION

Proposed Low Power Low Swing Clock Gated FlipFlop (LPLSCGFF) uses clock gating techniques that reduce power by deactivating the clock signal when there is no requirement for an effective switching. It also utilizes power reduction techniques like conditional capturing and use of reduced swing inverters at the clock port. This Flip Flop drastically reduces the noise compared to the existing flip flops. From all the three circuit simulation results, it is observed that the power consumption in a flip flop can be reduced considerably by implementing specifically designed clocking circuit. Low-swing resonant clock in a pulsed Flip-Flop results in a delayed Flip-Flop response. Low-swing sinusoidally clocked flip-flop can achieve further power reduction in LC resonant CDNs. The possibility of further power reduction in LPLSCGFF may be achieved by double edge triggering in the clocking scheme with low swing sinusoidal global clock signal.

It can be concluded that state elements equipped with conditional features have advantageous properties, particularly in low data activity conditions. Conditional techniques are suitable for the application in the high-performance VLSI circuits in the future. Several low power techniques, including low swing and clock gating, are incorporated into the new flip-flop to build low power clocking systems.In future it can be very suitable for System-On-Chip (SOC) applications which will lead us to a brighter tomorrow with low power consumption. This can be much suitable for application of battery oriented operation for less power and area. In future we can add some other leakage reduction techniques and the power can be further reduced

TABLE I
Power Consumption Comparison

Flip-Flop	Power Consumption	Noise Level	Total RMS Noise
CDMFF	33mW	260fV/√Hz	77.8pV
LSDCCFF	23mW	750fV/√Hz	235pV
LPLSCGFF	2.2mW	.024fV/√Hz	7.55fV

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