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RESEARCH ARTICLE

A COMPARATIVE STUDY OF VARIOUS ERROR CORRECTION CODES

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Abstract— Multiple cell upsets (MCUs) are the major reliability issue of memories, when exposed to radiation. To prevent the occurrence of MCUs several error correction codes (ECCs) are used, but the main problem is that they require complex encoder and decoder architecture and higher delay overheads. The decimal matrix code (DMC) minimizes the area and delay overheads compared to the existing codes such as hamming, matrix codes, built in current sensor etc, and also improves the memory reliability by enhancing the error correction capability.

Keywords— Multiple Cell Upsets (MCUs), Error correction codes (ECCs), Decimal matrix code (DMC), Matrix code (MCs), Reed muller code (RMC), Punctured deference set (PDS)

I. INTRODUCTION

The CMOS technology scaling to nm, low cost, high density, high speed integrated circuits with low supply voltage has increased the probability of fault occurrence in the memories. This lead to the major reliability concern especially increases SRAM memory failure rate. Some commonly used mitigation techniques are triple modular redundancy, and error correction codes (ECCs).

Soft errors are the major issue in the reliability of memories. Soft error will not damage the hardware, they only damage the data that is being processed. If detected, soft errors are corrected by rewriting corrected data in the place of erroneous data. Highly reliable system uses error correction approach, however in many systems it is difficult to correct data, or even impossible to detect error.To prevent soft errors from causing corruption in the data stored error correction codes are used such as matrix code, hamming etc. when ECC is used, data are

encoded when written in the memory and data are decoded when read from the memory. Thus the encoding and decoding process possess a vital impact on the memory access time and complexity.

Multiple cell upsets have become the reliability concern in some application apart from single cell upset. The BCH code,reed Solomon code etc are used to deal with MCUs,but the area,power and delay overhead of these codes are high due to the complex encoding and decoding architecture. The decimal matrix code uses encoder reuse technique which uses encoder as apart of the decoder and thus reduces the area overhead and complexity.DMC enchances the reliability of the memory by improving the error correction capability.

II. VARIOUS ERROR CORRECTION CODES

2.1 Hamming Code

Hamming code is a form of linear error correcting code that can detect up to two-bit error or correct one-bit errors without detection of uncorrected errors. By contrast, the simple parity code cannot correct errors but can only detect odd number of error bits. Hamming codes are prefect codes with minimum distance 3.

The hamming code is extended by adding a extra parity which will increase the minimum distance of the code to 4, which helps decoder to distinguish between single bit error and two bit error. Thus the decoder can detect and correct a single error and at the same time detect a double error. If the decoder does not attempt to correct errors it can detect upto three errors.

2.2 Reed Muller Codes

Reed muller codes (RMC) are the family of linear error correcting codes used in communication. It is listed as RM (d,r),where d is the order of the code and r determines the the length of the code,$n=2^r$. the block length is 2^m and distance is 2^{m-r}. Special case of reed muller codes includes the Hadamard code, the walsh-hadamard code, and Reed-solomon code.

The improved RMC decoding circuit proposed in[2], namely modified triple error RMC decoding circuit results in power saving,improved performance,less delay overhead. This provides protection againt any triple error. The use of ECC will improve the reliability but however this also increases the area overhead and access time. If no error correcting codes are used then it will result in less reliability and fault tolerance.

2.3 Difference Set Cyclic Code

The majority logic detector/decoder (MLDD) proposed in [3], uses a difference set cyclic code which is a part of LDPC. The DSCC has the property like larger error correction, modular encoding and decoding architecture which causes efficient hardware implementation. The interesting point of DSCC is that error detection is carried out in a simple way, using parity check sum. The code length is $N=2^{2S}+2^S+1$ and minimum distance is 2^s+2.

The result shows that this technique is capable of detecting up to five bit flips in the first three cycles. This improves the performance of the memeories compared to MLD.The error detecting module is independent of code size, hence the area overhead is less compared with the syndrome fault detection (SFD).

2.4 Built-In-Current Sensors

BICS are proposed to assist with single error correction and double error detection codes to provide protection against MCUs. However, this technique can only correct two errors in a word. The coupling of BICS with H-tree architecture proposed in [4], possess lower overheads, simple encoding and decoding algorithm and zero fault detection latency time.

The BICS is combined with either parity code or hamming code. When BICS is combined with the hamming code (BICS+H) ,called modified hamming code possess better reliability than the BICS combined with parity code. This approach corrects two random error per row in addition to MCUs. The overheads of BICS+P is 12% less than that of the hamming code and the modified hamming code with BICS has 5 times more reliable compared with the conventional hamming code.

2.5 Matrix Code

Matrix code discussed in [5], is the combination of hamming code and parity code which is proposed to improve the reliability and yield of memory chips against multiple cell upsets. Compared with reed muller the area is reduced by 25% and yield is found to be 300% better than Reed muller code. The code is presented in a matrix format where a n-bit word is divided into subword k1 and width k2(n=k1*k2). A(k1,k2) matrix is formed were k1 and k2 are rows and columns respectively. Matrix method provides detection and correction coverage somewhere in between the Hamming and Reed–Muller codes. However, the Hamming code is not adequate for more than two errors and the Reed–Muller imposes significant area and power consumption compared tothe proposed method.

III. PROPOSED WORK

3.1 Decimal Matrix Code

In this paper, decimal matrix code is proposed to provide enhanced memory reliability. This approach uses decimal algorithm, which increases the error detection capability. In the proposed work encoder is reused as a part of decoding circuit, thus reduces the area overhead compared to other techniques.

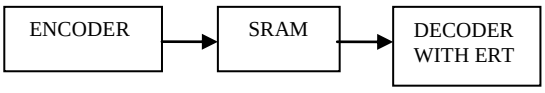

Fig 1.DMC based fault tolerent memory

3.2 Analysis of Area, Power and Delay

The area, power and delay of various error correction codes are compared and tabulated in table I.

TABLE I

AREA POWER AND DELAY ANALYSIS

ECCs	Area (μM^2)	Power (mv)	Delay (ns)
DMC	41572	10.8	4.9
MC	77933	24	7.1
PDS	486778	221.2	18.7
HC+BICS	137782	139	5
PR+BICS	120866	109.7	4.2
RMC	264602	264.8	5.5
HAMMING	58400	20.5	6.7

Table I shows that the proposed decimal matrix code possess lower area and power compared to the existing hamming, MCs, PDS etc.meanwhile the delay of the proposed code is greater than built-in-current sensor combined with parity code but less than other codes such as hamming ,MCs .

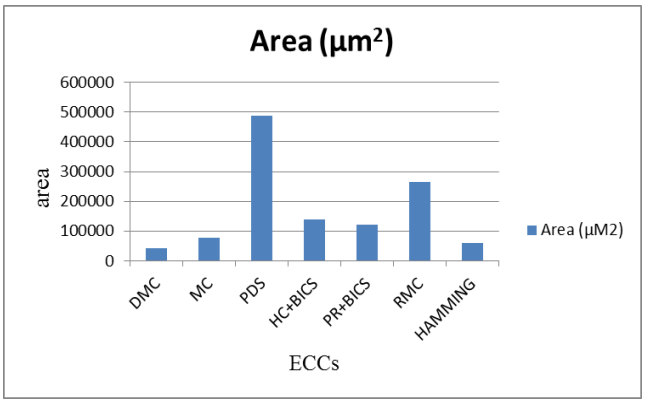

Fig 2. Area comparison of various ECCs

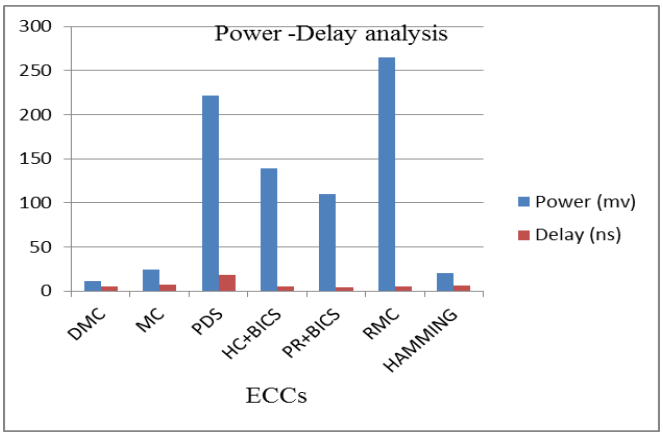

Fig 3. Power and delay comparison of various ECCs

IV. CONCLUSION

Error correction codes are used to improve the memory protection and make the memory fault free. The various ECC are used to detect the occurrence of error and also correct the detected ones; however the error detection capability and the overheads vary based on the codes used.

In this work decimal matrix code, is used which will possess higher memory protection and lower area and delay overheads. The only drawback in this approach is that the number of redundant bit is more. The future work is to reduce the number of redundant bit, without affecting the reliability of the memory.

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