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RESEARCH ARTICLE

Design and Implementation of Power Efficient Turbo Decoder

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ABSTRACT: Turbo decoding is viewed as superior alternate decoding technique in communication system, the circuit complexity and power consumption of turbo decoder implementation can often be prohibitive for power constrained system. To address these issues a power efficient turbo decoder based on soft out viterbi algorithm is designed. SOVA based turbo decoder can be implemented with high throughput and less complexity, This project work is towards Design and ASIC implementation of turbo decoder Using TSMC 65nm library, RTL model for Decoder is developed using HDL and synthesized, targeting ASIC implementation, clock gating technique has been adopted to meet low power requirement.

Keywords— turbo decoder, low power, soft out viterbi algorithm.soft-in soft out, ASIC

I. INTRODUCTION

The main intention of communication system is to provide uncorrupted data with less delay and power consumption. Demand for turbo code in wireless communication has been increasing since early 1990s, due to large coding gain various wireless standards such as 3GPP; HSDPA and WiMAX have adopted turbo codes.

fig .1 below illustrates the role of message passing in the decoding process.

Turbo codes are among the most powerful error correcting codes approaching very close to the Shannon's limit with a very large interleaver size [1]. To decode such codes, the maximum a posteriori (MAP) algorithm [2] was modified to be suitable for decoding recursive systematic convolutional (RSC) codes in an iterative process.

Two Algorithms maximum a posteriori (MAP) and soft-out viterbi algorithm (SOVA) are two widely used turbo decoder implementation. In terms of bit error rate (BER) MAP based turbo decoder give better performance but their complexity and latency is very high, because of high complexity gives large delay which prevent the use of turbo code in real time application.

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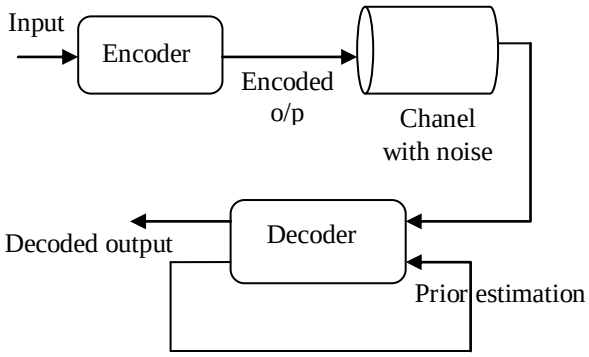

Fig .1 Message Passing from transmitter to receiver

The SOVA based turbo decoder can be implemented with high throughput, less complexity, with the increase in demand for real time application, this need coupled with emergence of device that perform decoding in software, that led to come up with a software based turbo decoding scheme that has a performance close to that of SOVA, while it greatly reducing complexity and Leeds to less delay and power consumption.

In this paper section II explains the turbo encoder and gives the general block diagram of turbo encoder, in section III brief out the turbo decoding techniques and their classification, section IV explains the iterative SOVA turbo decoding, section V gives the ASIC implementation and section VI gives simulation result and power comparison of turbo decoder using clock gating technique and without using clock gating technique is tabulated and paper is concluded in section VII.

II. TURBO ENCODER

The general structure of turbo encoder is shown in fig.2 .It consists of rate 1/3 parallel concatenated turbo code. encoder consists of two rate ½ recursive systematic convolutional encoders .it should be note that both are identical ,these encoders are called of parallel concatenation because both encoders are operate on same set of input bits rather than one encoding the output of other as in the case of serial.

The first encoder receives un-coded data bits in natural order and outputs a set of parity bits, the second component encoder receives a permutation of the data bits from a block interleaver and outputs a second set of parity bits.

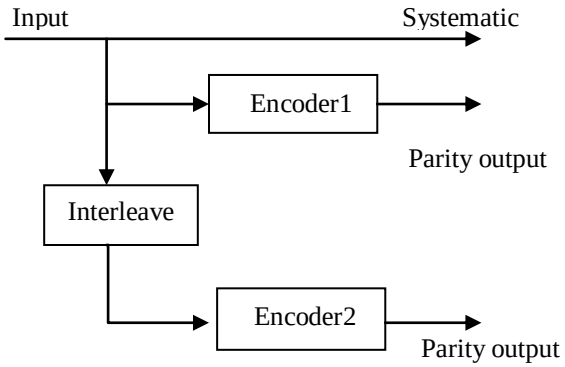

Fig.2 Turbo encoder

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III. DECODING OF TURBO CODES

Various decoding algorithm available for decoding turbo codes, all the turbo decoding algorithms are based upon trellis based estimation. The trellis based estimation algorithms are classified into two type's sequential estimation algorithms and symbol- by-symbol estimation algorithm.

The viterbi algorithm, SOVA and improved SOVA algorithm are classified as sequential estimation algorithm, where MAP, max-log-map and log-MAP are classified as symbol-by-symbol estimation algorithms. In general MAP, log-MAP, max-log-MAP, SOVA and improved SOVA, all these algorithms produce soft output. The viterbi algorithm is a hard-decision decoding algorithm; SOVA is a soft-out producing viterbi algorithm.

However on practice MAP turbo decoder is too complex to be implemented because of large number of multiplication and need of non-linear function, for that reason two simplified versions of it were Log-MAP and Max-Log-MAP[3], latter is sub-optimal in terms of BER performance but easier to implement requires only addition and max operator.

Another sub-optimum algorithm suitable for turbo decoding is soft output viterbi algorithm. It was found that the iterative SOVA is 0.7dB worse than the MAP algorithm at BER of IO4 *[3]*. This is because the SOVA considers only two path sequences to update its soft output, namely the survivor and the concurrent path sequences; fig 3 below shown is the turbo decoder.

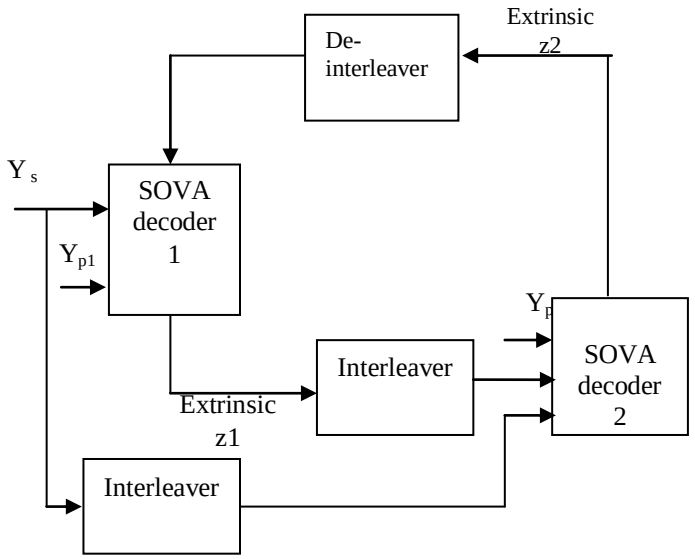

Fig.3 Turbo decoder

Block interleaver; helical interleaver and pseudo random interleaver are widely used different kinds of interleavers suitable for turbo decoding,

Block interleaver write data in row wise and read data in column wise, in helical interleaver it reads data in diagonal form, in pseudo random interleaver here it write data in i^{th} and read data at j^{th} address.

IV. THE ITERATIVE SOVA

The SOVA is based on the classical process of the VA**,** Followed by an updating rule to produce soft outputs on the estimated bit sequence.

At an instant time k the VA finds the survivor path, which is the path that has the smallest path metric between all the Metrics of paths that enter each state. The path metric is the Summation of all the branch metrics

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of a state sequence, to do this, we define the branch metric between two states of a path, based on the squared Euclidean distance, as

$$\lambda_k = \sum_{i=0}^{n-1} \left(y_{k,i} - x_{k,i}\right)^2$$

where *l/n* is the code rate, *n* is the codeword size, xk,; is the i-th transmitted symbol (or bit assuming BPSK modulation) and yk,i is the corresponding received value at the receiver

When the process of the VA has finished, only two paths are needed for the SOVA, the survivor or the best path and its Strongest competitor path, that is the path which had diverged at a past time k-v and merged to the same state as the survivor path at time *k*, their path metric difference A is also stored and the process of the SOVA is starting from the Last state of the trellis by tracing back.

To produce the bit Log Likelihood Ratio (LLR) values, we first initialize all the reliabilities of the survivor sequence to
L, = +∞ and then we update as

$$Ls = \min (Ls, \Delta), \text{ if } \mathbf{u_s} \neq \mathbf{u_c}$$

Where L_S is another reliability value representing the concurrent path, that additional updating rule makes the BR superior compared to the HR.

The power efficient turbo decoder based on SOVA will be implemented using clock gating and by using low power cadence library.

V. ASIC IMPLEMENTATION

The synthesized RTL schematic of top level Designed Turbo Decoder using RTL compiler is show in the Fig 4, it has decoder, interleaver and de-interleaver blocks, the Clock gating technique is used to meet the low power requirement of the design.

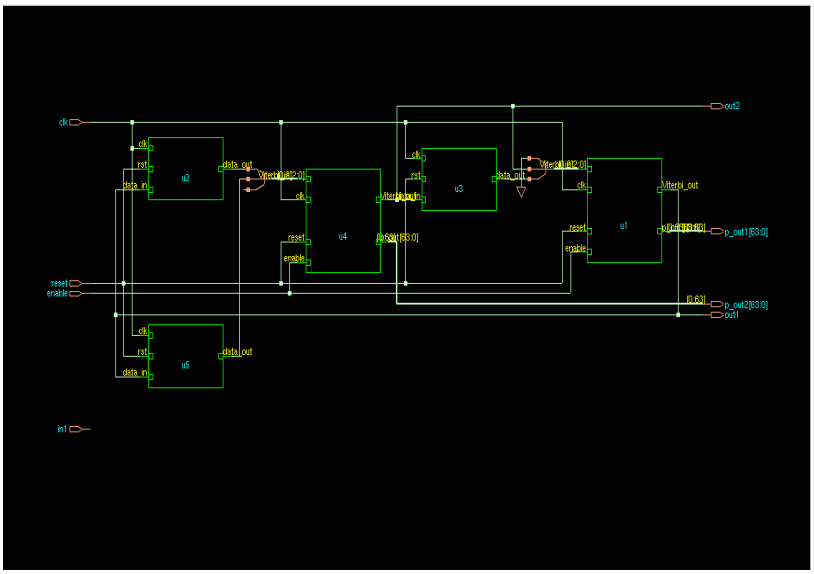

Fig 4 RTL schematic of turbo decoder

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a. Hardware model

The final design after implementation of turbo decoder is shown in fig 5.

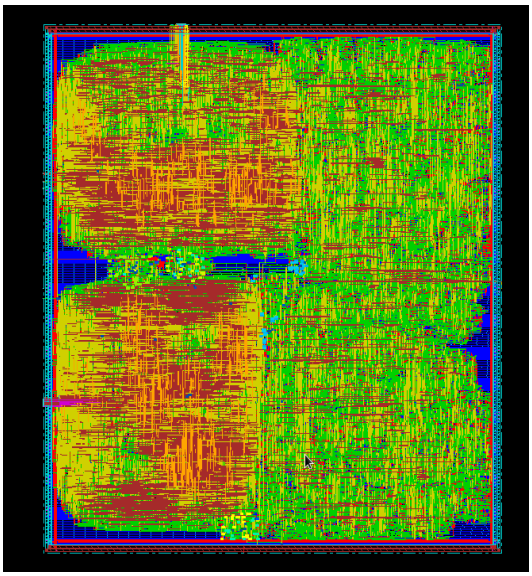

Fig 5 Turbo Decoder design after implementation

Standard cells placed in the core, pins and the routing of signal is shown, for turbo decoder after ASIC implementation.

VI. RESULT

Simulation result for SOVA based turbo decoder is shown in fig.6; designed is simulated using Xilinx ISE 14.1 at 200 MHz frequency.

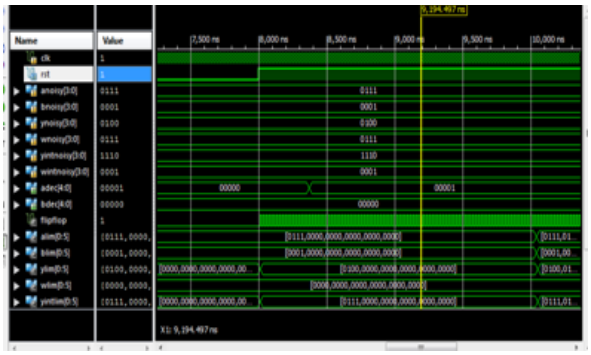

fig.6 simulation result for SOVA based turbo decoder

From the below table1 it shows that the design with clock gating consumes 13.09mW and design without clock gating consumes 17.31mW that is the design with clock gating consumes 24.37 % less power compared to design without clock gating.

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Turbo decoder	Without clock gating in mW	With clock gating in mW
Total internal power	10.37	7.622
Total Switching Power	6.938	5.461
Total Leakage Power	0.008928	0.007605
Total Power	17.31	13.09

Table1 Power comparison

VII. CONCLUSION

In this paper we have present a turbo decoder based on soft out viterbi algorithm, SOVA decode algorithm provide the reduced complexity necessary for hardware implementation. Simulation result for SOVA based turbo decoder is verified.

The power efficient turbo decoder is implemented using clock gating technique and Reduce the power consumption of the design by 24.37 % at clock frequency of 200MHz.the design is synthesized using cadence RTL compiler and physical design is done by using cadence soc encounter.

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