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PERFORMANCE ANALYSIS OF AN EFFICIENT PULSE-TRIGGERED FLIP FLOPS FOR ULTRA LOW POWER APPLICATIONS

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Abstract: Major portion of the on-chip power is stirred by the clock distribution network and flop-flops. In synchronous systems, High speed can be achieved using different sophisticated Pipelining techniques. A novel ultra-low-power pulse-triggered flip flop is designed and simulated by reducing the number of transistors stacked along the discharging path by including a two-input pass transistor logic (PTL)-based AND gate to control the discharging path of the transistor. Also performance analysis is done by comparing with the existing conditional pulse-enhancement scheme designs such as implicit-Data Close to Output (ip-DCO), modified hybrid latch flip-flop (MHLFF), single ended conditional capturing energy recovery(SCCERR).

Keywords: Pulse triggered flip-flops, Pipelining, ultra low-power, pass transistor logic, on-chip power.

I. INTRODUCTION

In all types of digital circuits design, the basic elements are Flip-Flops (FFs) which are used extensively nowadays. Specifically digital designs utilize intensive pipelining techniques and adopt many different Flip-Flop modules. The power consumption of clock system which consists of clock distribution networks and storage elements is high of the total system power [1]. In recent VLSI's clock distribution systems, Pulse triggered-FF (P-FF) has been considered a popular alternative to the conventional master slave based FF in the application of high speed operations [2].

High performance flip flops are essential key elements in the design of high-speed integrated circuits. An efficient pipeline technique in which only few logic levels are inserted between pipeline stages to obtain high clock frequencies. In this paper, we present novel ultra low-power P-FF design, features a conditional pulse-enhancement scheme. To support this feature three additional transistors are employed. In spite of increase in total transistor count, transistors of the pulse generation logic scheme benefit from significant size reductions and the overall layout area is even slightly reduced.

II. LITERATURE SURVEY

Conventional Pulse Control Scheme Pulse triggered-FF (P-FF) Designs

A. *implicit-Data Close to Output* (ip-DCO)

ip-DCO is known as the implicit data close to output. It is an implicit type flip-flop. In this method the pulse is generated inside the flip-flop. A state-of-the-art P-FF design, named ip-DCO, is given in Figure 2.1 [3].

It contains an AND logic-based pulse generator and a semi-dynamic structured latch design. Semi-Dynamic Flip-Flop is a high performance flip-flop because of its small delay and simple topology. It is measured to be one of fastest flip-flops today.
Inverters I5 and I6 are used to latch data and inverters I7 and I8 are used to hold the internal node X. The pulse generator takes complementary and delay skewed clock signals to generate a transparent window equal in size to the delay by inverters I1-I3. Two practical problems exist in this design. First, during the rising edge, nMOS transistors N2 and N3 are turned on. If data remains high, node X will be discharged on every rising edge of the clock. This leads to a large switching power.

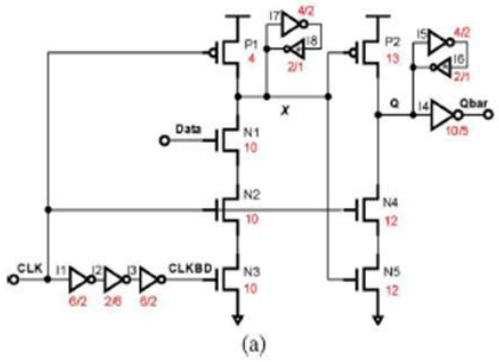

Fig 2.1: ip-DCO

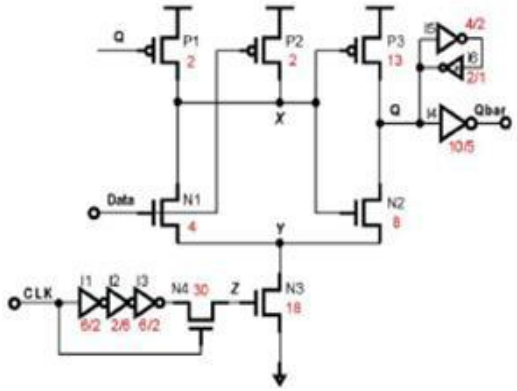

Fig 2.2: MHLLF

B. *Modified Hybrid Latch Flip-Flop* (MHLFF)

The modified hybrid latch flip-flop is known as MHLFF and this is a type of implicit type flip-flop.

MHLFF shows an improved P-FF design in fig.2.2 [5]. It employs a static latch structure. A static latch can remember as long as gate power is supplied. It uses feed-back to remember, rather than depending on the charge on a capacitor. Node X is no longer precharged periodically by the clock signal. A weak pull-up transistor P1 controlled by the FF output signal Q is used to maintain the node level at high when Q is zero.

This design eliminates the unnecessary discharging problem at node. However, it encounters a longer Data-to-Q (D-to-Q) delay during "0", "1" transition because node is not pre-discharged. Larger transistors N3 and N4 are required to enhance the discharging capability. Another drawback of this design is that node becomes floating when output Q and input Data both equal to "1". Extra DC power emerges if node X is drifted from an intact"1".

C. Single Ended Conditional Capturing Energy Recovery (SCCER)

SCCER is known as the single ended conditional capturing energy recovery P-FF shown in figure 2.3 [7]. It is a refined low power PFF design using a conditional discharged technique. This technique is also used to present a new flip-flop Conditional Discharge flip-flop (CDFF) [4], [7].

CDFF use a pulse generator which is suitable for double edge sampling. CDFF has two stages. First is responsible for capturing the Low-to-High transition and second stage captures the High-to-Low input transition. In this SCCER design, the keeper logic is replaced by a weak pull up transistor P1 in conjunction with an inverter I2 to reduce the load capacitance of node.

The discharge path contains nMOS transistors N2 and N1 connected in series. In order to eliminate superfluous switching at node, an extra nMOS transistor N3 is employed. Since N3 is controlled by Q_fdbk, no discharge occurs if input data remains high.

The worst case timing of this design occurs when input data is "1" and node is discharged through four transistors in series, i.e., N1 through N4, while combating with the pull up transistor P1. A powerful pull-down circuitry is thus needed to ensure node can be properly discharged. This implies wider N1 and N2 transistors and a longer delay from the delay inverter I1 to widen the discharge pulse width.

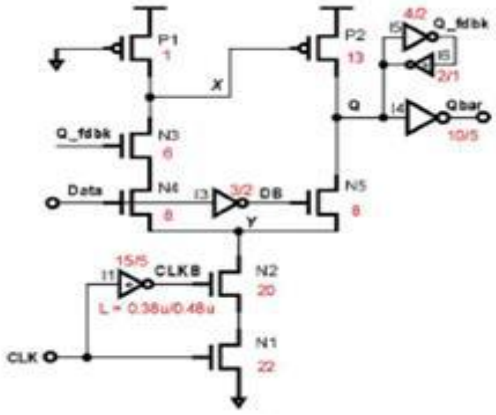

Fig 2.3: SCCER

III. PROPOSED MODEL

The proposed model is an implicit type pulse triggered flip-flop (P-FF) with a conditional pulse enhancement scheme. To overcome the draw backs in the conventional designs two measures are employed. In the conventional designs delay is high and also large power is consumed because of presence of the large number of transistors in the discharge path and also large power is consumed in power-up of the transistors. So, the number of n-type MOS transistors (NMOS) in the discharging path should be minimized. Also there is a need to increase the pull down strength when the input data is high i.e., data=1. So there is a need to conditionally enhance the pull down power when input data is "1." This design takes the concept of the SCCER design. Transistor stacking design of ip-DCO in figure 2.1 and SCCER in figure 2.3, is replaced by removing the transistor N2 from the discharging path. Transistor N2 and N3 are connected in parallel to form a two-input pass transistor logic (PTL)-based AND. It controls the discharge of transistor N1. The input to the AND logic is complementary to each other so the output node is kept at zero. There is a floating node when both input signals equal to "0". But it doesn't effect the circuit performance. The critical condition occurs only when there is rising edges at the clock pulse. Transistors N2 and N3 are turned ON together in this case to pass a weak logic high to node. This weak pulse strength is enhanced by switching ON the transistor N1 by a time span equal to the delay provided by inverter I1. The switching power at node can be reduced due to a diminished voltage swing. Unlike the MHLLF design, where the discharge control signal is driven by a single transistor, parallel conduction of two n-type MOS transistors (N2 and N3) speeds up the operations of pulse generation.

Designing the flip-flop like this, the number of transistors in the discharge path can be reduced. Also the pulse generation speed increases and then delay is reduced. The area overhead is also reduced. The flip-flop using the conditional enhancement scheme is given in the figure 3.1.

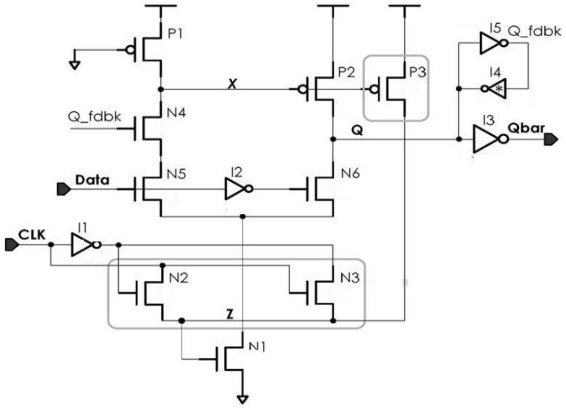

Fig 3.1: Proposed Model

Pulses that trigger discharging are generated only when there is a requirement, so unwanted circuit activity due to glitches can be minimized which reduces the overall power consumption and pulse discharge can be fast. The delay inverters which consume more power for stretching the pulse width are replaced by the P-type MOS transistors which enhances the pull down strength when there is a longer discharge path. Transistor sizes are also reduced to provide area and power saving.

IV. SIMUATION RESUTS

Simulation results are shown in given figures and window appears with inputs and output. The power consumption is also displayed on the right bottom portion of the window. By changing the transistor sizes, different layout designs can be generated with different target delays. Depending on the input sequences assigned at the input and the output is observed in the simulation.
To demonstrate the proposed design, post layout simulations on various P-FF designs were conducted to obtain their performance analysis. These designs include the three P-FF designs shown in figures 4.1a and 4.1b of ip-DCO circuit and waveforms, figures 4.2a and 4.2b of MHLLF circuit and waveform, figure 4.3a and 4.3b of SCCER circuit and waveform are simulated results using 90-nm CMOS process, and figure 4.4a and 4.4b of proposed P-FF design is simulated results using 45-nm CMOS process. The operating condition used in simulations is 500 MHz and 1.0V. All designs are further optimized subject to the tradeoff between power and delay i.e., minimizing the product of the two terms (Data to output delay (D-to-Q) and power).

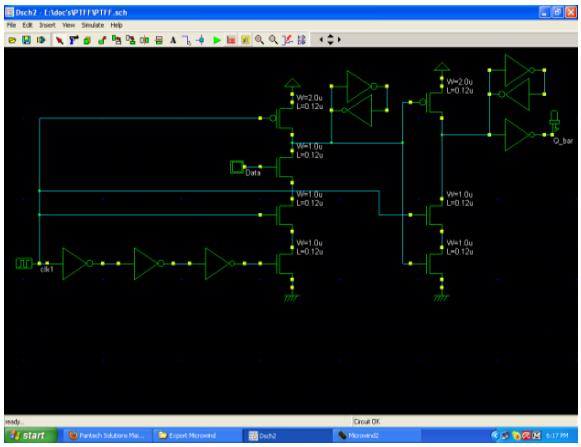

Fig: 4.1 (a) ip-DCO Cicuit

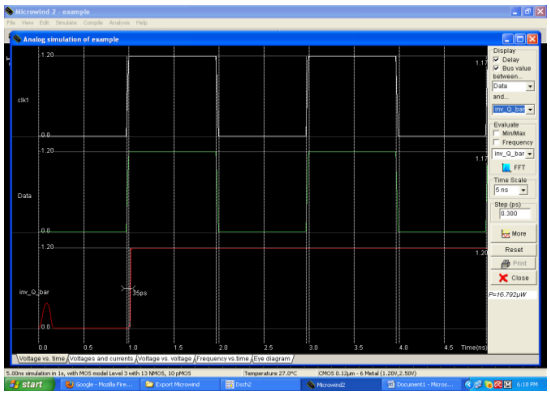

Fig: 4.1(b) ip-DCO waveform

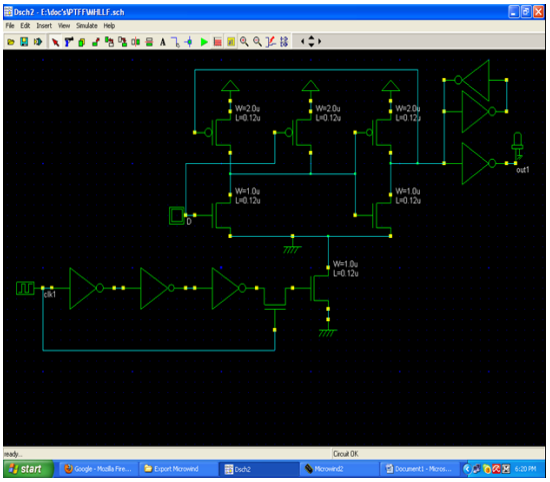

Fig: 4.2(a) MHLLF Circuit

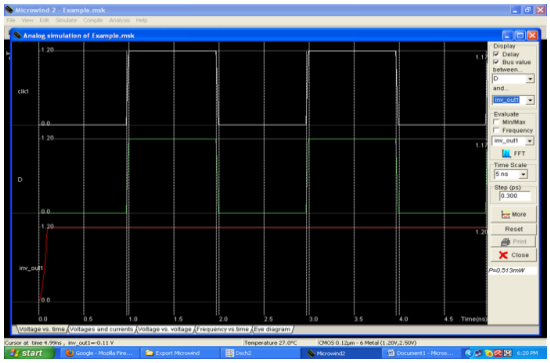

Fig: 4.2(b) MHLLF waveform

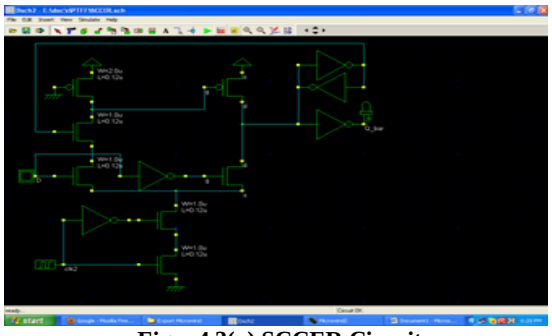

Fig: 4.3(a) SCCER Circuit

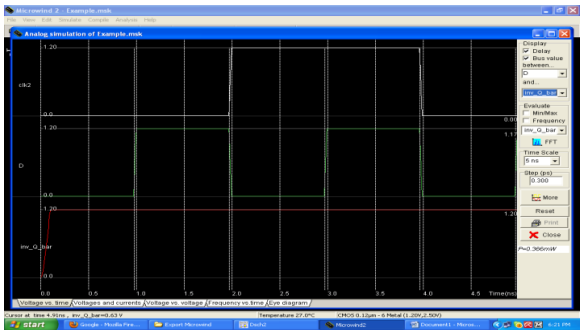

Fig: 4.3(b)SCCER waveform

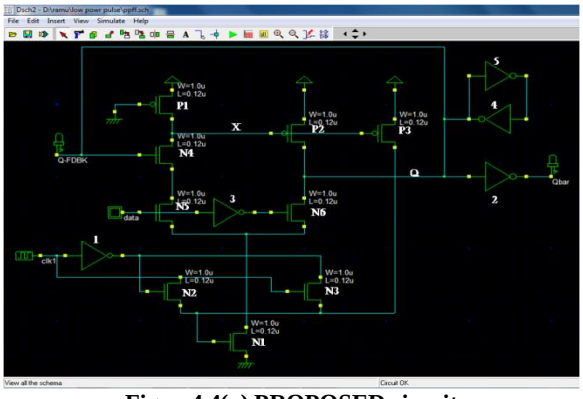

Fig: 4.4(a) PROPOSED circuit

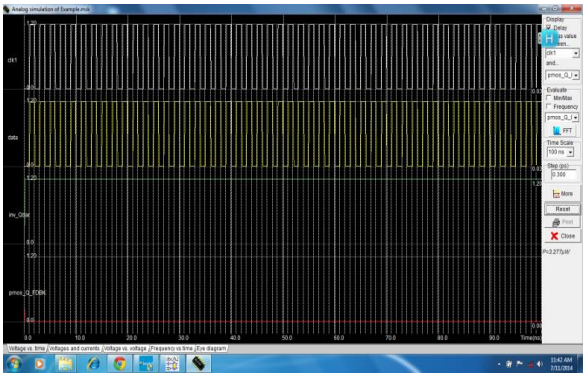

Fig: 4.4(b) Proposed System waveform

Above mentioned representations are the simulated blocks of ip-DCO, MHLLF, SCCER and proposed concept in Microwind software package.

V. PERFORMNACE ANALYSIS

According to the mentioned designed methods, the various parameters are tabulated and analyzed. With this performance analysis results the Proposed P-FF design performed better than other designed methods

Table 5.1: Performance Analysis of different designs.

P-FF	IP-DCO	MHLFF	SCCER	PROPOSED
No. of transistors/ Layout area (µm2)	23/91.88	19/93.02	17/80.07	19/79.17
Avg. Power (µW)	16.97	51.7	36.6	3.277

VI. CONCLUSION

In this paper, a ultra low-power pulse-triggered flip-flop (FF) design is presented. In this the clock generation circuitry an AND function is removed and is replaced with a Pass-Transistor logic based AND gate. Since in the PTL-style AND gate the n-mos transistors are in parallel they consume less power and provides a faster discharge of the pulse. The power consumption shows a decreasing trend as the switching activities are minimized .From the above results it is clear that this type of design approach can be implemented in real space systems to increase the efficiency as well as to minimize the power consumption.

VII. FUTURE SCOPE

Dual edge triggered flip-flop can be designed in future. By designing the clock generation circuit that will operate in both positive and negative edge triggering of the clock pulse. This method overcomes the single edge triggering and also reduces the power consumption.

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