Available Online at www.ijcsmc.com

International Journal of Computer Science and Mobile Computing

A Monthly Journal of Computer Science and Information Technology

ISSN 2320–088X
IMPACT FACTOR: 6.017

IJCSMC, Vol. 6, Issue. 8, August 2017, pg.32 – 35

DYNAMIC LATCH BASED COMPARATOR

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Abstract: High speed analog to digital converters (ADC), memory sense amplifiers, RFID applications, data receivers with low power and area efficient designs has attracted a wide variety of dynamic comparators. This paper presents an improved design for a dynamic latch based comparator in achieving lower power dissipation. The comparator has two different stages comprising of a dynamic differential input gain stage and an output latch. The objective of improving the speed of conversion is done by removing the dead time required for reset in the differential input stage. In the proposed work the output node in the differential gain stage requires lesser time to regain higher charge potential. The proposed methodology has been designed and simulated using 180nm technology operated on a single 1.8V power supply and achieves complete conversion in nsec.

Keywords: analog to digital converter, dynamic clocked comparator, dynamic latched comparator

I. INTRODUCTION

Comparators are considered to be one of the rudimentary building-blocks in most ADCs. Major criterion for a comparator design is high speed, low power and lesser real estate over the chip [1]. Figure 1 shows the conventional latched-based-comparator, a small input-voltage difference at the input terminals is pulled up to a full scale digital level in a short-span of time, by a positive-feedback mechanism (regenerative-latch). Due to the random offset errors and internal parasitic/external load capacitances mismatches they suffer a lot of accuracy issues. To overcome this inaccuracy issue, the conventional architecture used a separate pre-amplifier stage anteceding the positive feedback-stage due to which it could amplify a small difference in the input-voltage to a full scale digital output, negating the kickback noise [3]. But for a electronic devices with a feature of high-speed and low-power application, a comparator without the pre-amplifier is preferred since it suffers from high static power dissipation.

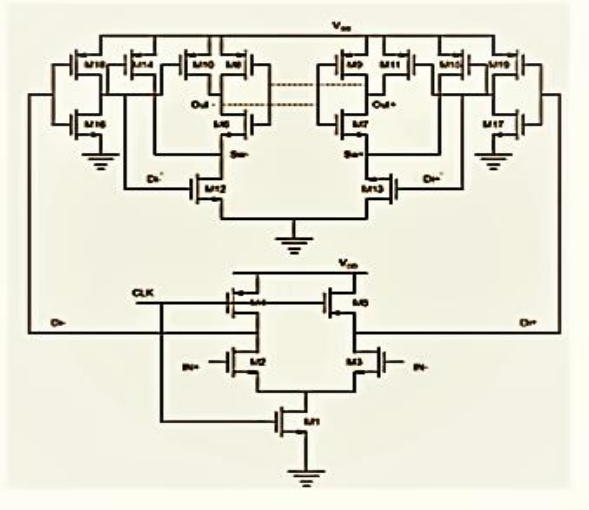

Fig No 1. Conventional latch based comparator

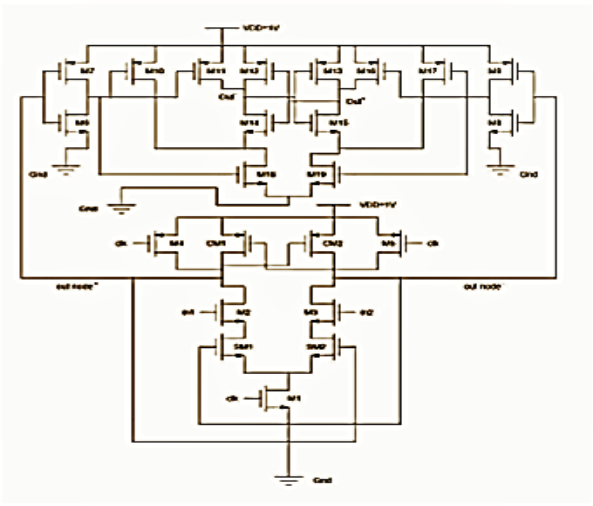

Fig 2. Proposed dynamic latch based comparator

The present work deals with increasing the speed of comparison of a comparator which is done by incubating a modified dynamic-latch-based-comparator as proposed. In the reset-phase the output nodes has to be charged up to the initial supply voltage level. This charging of the output nodes induces latency in the process of comparison. We propose a modified approach to tackle this dead time required to reset and improve the speed of comparison.

II. Methodology

1. Conventional Latch Based Comparator

In the conventional approach, the output nodes was just the function of input transistor transconductance and input voltage difference. This created a timing constraint during the next reset phase due to fact that the output node capacitances was again needed to be charged back to VDD. Extra two nMOS transistors SM1 and SM2 acting as switches are also used in the proposed work to avoid the direct consumption of current from VDD to ground through the tail transistor M1 resulting in saving static power consumption. The design does not use any specific low voltage transistors. The current flowing through the input transistors M2 and M3 of the differential gain stage can be related from Eq. 1 and Eq. 2.

$$V_{Di-}(t) = V_{DD} - \frac{I_{D2}}{C_{Di-}}t \qquad (1)$$

$$V_{Di+}(t) = V_{DD} - \frac{I_{D3}}{C_{Di+}}t \qquad (2)$$

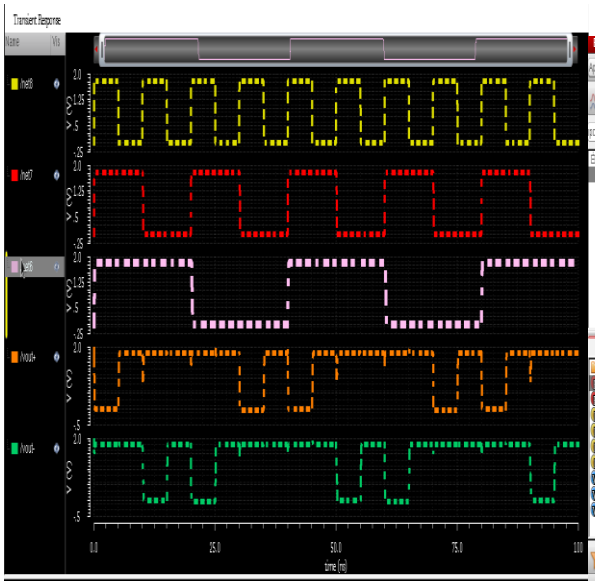

Fig 3 Wave form of latch based comparator

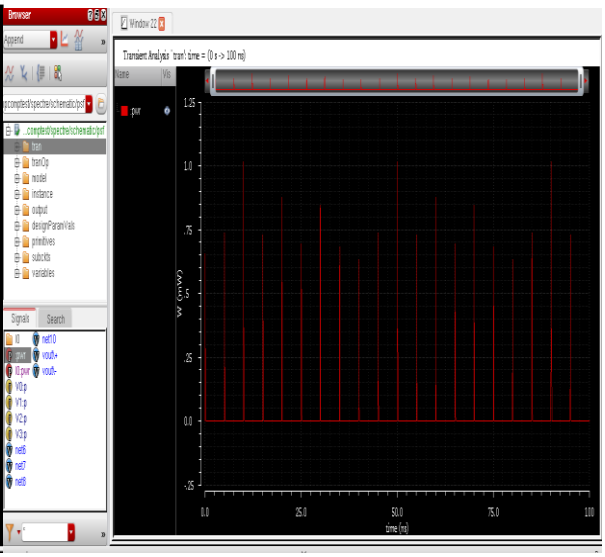

fig 4 Power dissipation of latch based comparator

Problem with latch based comparator

The major pitfall of comparator design is the dead time required to reset the output nodes of the differential gain stage back to supply voltage. Since the circuit has to wait for the next reset phase it significantly requires a larger time to charge the output node capacitances. This will slower the process of comparison which limits the speed of the comparator.

2. Dynamic latch based comparator

The proposed design is shown in Figure 2. It retains all important features of a comparator as can be obtained, beside offering high speed and removing dead time issue. It differs from Figure 1 with respect to the switching transistors SM1, SM2 which avoids dynamic power consumption and the control transistor CM1,CM2 which provides a extra mechanism to keep either of the outputs in the differential pair charged up to VDD. The two cross coupled control transistors CM1 and CM2 are used which at the beginning of the reset phase (clk=0) are turned OFF since pMOS transistors M4 and M5 pre-charge the output node to VDD. During the evaluation phase (clk=1) the tail transistor nMOS M1 turns ON and the output nodes start to drop at different rates based on the input voltages at transistors M2 and M3. The higher input voltage transistor will draw more current which drops the voltage at its drain terminal, turning ON either of the control transistors high keeping one control transistor completely OFF. This arrangement will make one of the output terminal discharge completely to the ground potential and keeps the other output node at a higher potential.

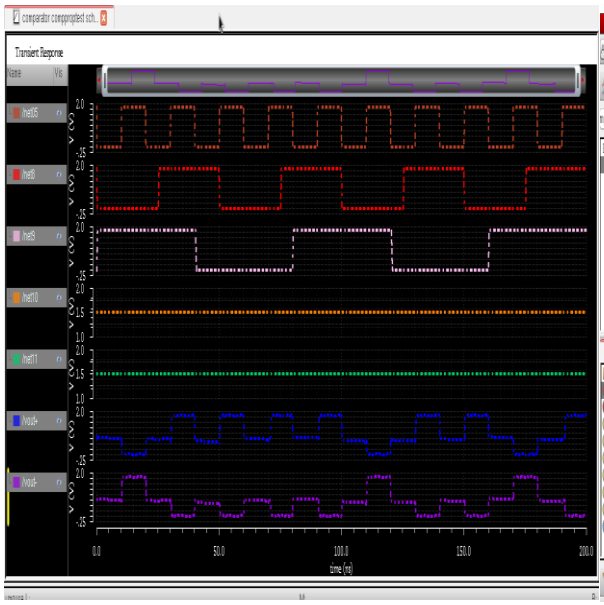

Fig 5 Simulation of DLC

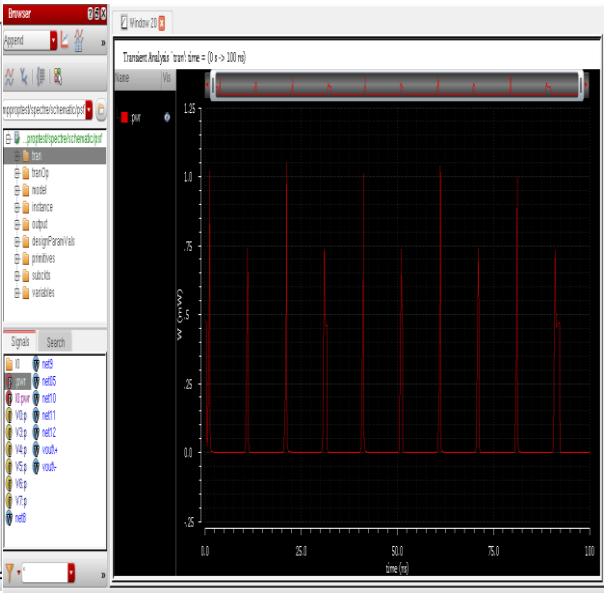

Fig.-6 Average power dissipation of DLC

III. Comparison with other work

PARAMETERS	Conventional logic	Proposed logic
1)Power(uW)	10.01uW	8.801uW
2)delay(ns)	30.3	22.1
3) Chip area	More	Less
4)Number of transistors used	19 Transistors	13 Transistors

Fig no 11. Comparison table

IV. Conclusion

The proposed work presents an improved dynamic latch based comparator. The dead time required to reset the output nodes was removed by making use of the proposed architecture in the input differential gain stage. This results in improved process of comparison and it also accelerated conversion process of the analog to digital converters. The static power dissipation was saved by using extra switches. Dynamic latched comparator was designed that works with high speed and low power consumption when compared to double tail latched comparator (conventional comparator 1) and pre amplifier based latch comparator (conventional comparator 2). For comparison we provide analog input to the comparator and the output will be digital. The simulation results show that the proposed circuit can operate at higher speed with low power dissipation than the other two comparators.

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