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RESEARCH ARTICLE

PV System with Virtual DC Bus for Cost Effective Grid Supply for Commercial Purpose

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Abstract: The main objective of this project to control the common mode leakage current by using virtual dc bus with PV systems. The power which we receive form the PV panel is not a constant supply due to various condition. In order to overcome this issue we are using Buck Boost converter for generating constant voltage supply to the inverter. The negative pole of the dc bus is connected directly to the neutral line of grid and the stray capacitance between the PV panels and ground is bypassed. Due to this, the common mode ground leakage can be suppressed completely. The negative voltage level for the negative ac grid current generation is achieved by virtual dc bus. Consequently the required dc bus voltage is same as full bridge inverter. Because of this concept a transformer less inverter is derived in which the virtual dc bus is realized with the switched capacitor technology. It consists of five IGBT power switches for controlling the voltage and two capacitors, single filter inductor and Buck Boost Converter. This PV systems with Virtual dc bus is modulated with unipolar sinusoidal pulse width modulation (SPWM) and the double frequency SPWM to reduce the output ripple current. Magnetic losses are controlled by a smaller filter inductor in this system.

Keywords— Shared approach (SA) current; photovoltaic (PV) system; switched capacitor; transformer less inverter; unipolar sinusoidal pulse width modulation (SPWM); virtual dc bus

I INTRODUCTION

The dispersed photovoltaic power generation systems have conventional increasing popularity in both the commercial and residential areas. In most occasions, the inverters are used to feed the PV power into the utility grid. It is significant for the PV inverter to be of high competence owing to the comparatively high price of the PV panels

[4]. Small size is also strongly desired for the low-power and single-phase systems, especially when the inverters are installed indoor. In the outdated grid-connected PV inverters, whichever a line frequency or a high-frequency transformer is utilized to provide a galvanic isolation between the grid and the PV panels. Eliminating the isolation transformer can be an effective solution to increase the efficiency and reduce the size and cost [6]. However, if the transformer is omitted, the common-mode ground leakage current may appear on the parasitic capacitor between the PV panels and the ground [7], [8]. The reality of the shared mode current may reduce the power conversion competence rise the grid current distortion, deteriorate the electric magnetic compatibility, and more importantly, give rise to the safety threats [9]. The common mode current path in the grid-connected transformer less PV inverter system is illustrated in Fig. 1. It is molded by the power switches, filters, ground impedance Z_G, and the parasitic capacitance C_{PV} between the PV panels and the ground. According to [10], the CM current path is equivalent to an *LC* resonant circuit in series with the voltage. The CM voltage v_{CM} is defined by

$$v_{CM} = v_{AO} + v_{BO}/2 + (v_{AO} - v_{BO})\, L_2 - L_1/2(L_1 + L_2)$$

where v_{AO} is the voltage difference between points A and O, v_{BO} is the voltage difference between points B and O, and L_1 and L_2 are the output filter inductors. If the switching action of the inverter generates high frequency CM voltage, the CM current *i*CM may be exited on the *LC* circuit. As of this fact of view, the topology and modulation strategy adopted for the transformer less PV power system must guarantee that *v*CM is constant or only varies at low frequency, such as 50 Hz/60 Hz line frequency. A simple way to realize this goal is to use the full-bridge inverter with the bipolar sinusoidal pulse width modulation (SPWM), of which the shared approach voltage is fixed at half the dc bus voltage. Relating with the bipolar SPWM, the unipolar SPWM has better performance in terms of the output current ripple and switching losses, but cannot be directly used for the full-bridge inverter in the transformer less application, because it generates the switching frequency CM voltage.

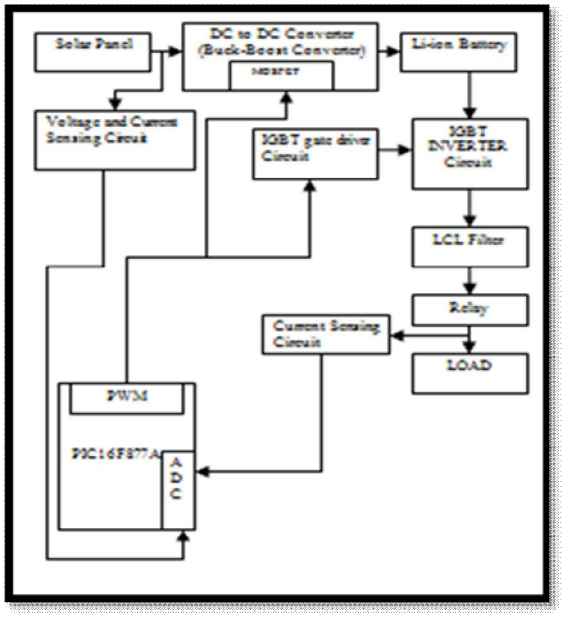

Fig 1. Functional Block Diagram

For this reason, some state-of-the-art topologies, such as the H5 inverter, the HERIC inverter, etc., have been developed based on the full-bridge inverter, to keep *v*shared method constant when the unipolar modulation is used [11]–[16]. Particular of these topologies are exhibited. By introducing extra switches into the full bridge inverter either on the dc or ac side, the dc bus can be disconnected from the grid when the inverter output voltage is at zero voltage level, so that the common approach current path is cut off. Such explanations need two filter inductors with independent iron cores, which may lead to a rise in the size and cost. Moreover, the dc and ac sides cannot be perfectly disconnected by the power switch because of the switch parasitic capacitance, so the CM current may still

exist [10]. One more kind of solution is to use the half-bridge inverter with the grid neutral line directly connected to the midpoint of the dc bus, In this method the voltage across the parasitic capacitor is clamped to be constant by the dc bus capacitor. However, this method has an important disadvantage that the required dc bus voltage should be doubled compared with the full-bridge topologies. For the 220 Vac system, it can be as high as 700 V. Although the three-level neutral point clamped (NPC) circuit can help improve the performance of the half-bridge inverter, the dc bus voltage is still high [17], [18]. Besides the aforementioned classic circuits, there are other topologies proposed in recent literature works. The Karschny inverter [19] and the paralleled buck inverter [20] are derived from the buck–boost and buck circuits, respectively. These solutions have high reliability, but are not capable of supplying the reactive power to the grid. The inverter proposed in [21] employs a capacitor voltage divider to keep the shared approach voltage constant, but is regarded to be of higher conduction losses.

In this paper, a original topology generation strategy called the virtual dc bus idea is proposed for the transformer less grid linked PV inverter. In this explanation the grid neutral line is connected directly to the negative pole of the dc bus, so that the voltage across the parasitic capacitor is clamped to zero. As a result, the shared approach current is eliminated completely. Meanwhile, the virtual dc bus is created to help generate the negative output voltage. The required dc bus voltage is still the same as the full-bridge, and there is not any limitation on the modulation strategy since the shared approach current is removed naturally by the circuit structure. In this way, the advantages of the full-bridge- and half bridge-based solutions are combined together. Founded on the aforementioned innovative idea, a novel inverter topology is proposed with the virtual dc bus concept by employing the switched capacitor technology. The future inverter can be modulated with the unipolar SPWM and double frequency SPWM. It consists of only five power switches and a single filter inductor, so the cost of the semiconductor and magnetic components can be reduced. This paper is organized as follows.

II VIRTUAL DC BUS CONCEPT

The concept of the virtual dc bus is portrayed. By linking the grid neutral line directly to the negative pole of the PV panel, the voltage across the parasitic capacitance *C*PV is clamped to zero. This prevents any leakage current flowing through it. By high opinion to the ground point N, the voltage at midpoint B is either zero or +*V*dc, according to the state of the switch bridge. The purpose of introducing the virtual dc bus is to generate the negative output voltage, which is necessary for the operation of the inverter. If a proper method is designed to transfer the energy between the real bus and the virtual bus, the voltage across the virtual bus can be kept the same as the real one. As shown in Fig. 6, the positive pole of the virtual bus is connected to the ground point N, so that the voltage at the midpoint C is either zero or −*V*dc. The dotted line in the figure indicates that this connection may be realized directly by a wire or indirectly. Supplementary transformer less inverter topologies: (a) Karschny inverter [19]; (b) paralleled-buck inverter [20]; (c) H6 inverter with capacitor voltage divider [21]. power switch. With points B and C joined together by a smart selecting switch, the voltage at point A can be of three different voltage levels, namely +*V*dc, zero, and −*V*dc. Meanwhile the CM current is removed naturally by the structure of the circuit; there is not any limitation on the modulation strategy, which means that the advanced modulation technologies such as the unipolar SPWM or the double-frequency SPWM can be used to satisfy various PV applications.

III RESULTING TOPOLOGY AND MODULATION APPROACH

Founded on the virtual dc bus concept, a novel inverter topology is derived as an example to show the clear advantages of the proposed methodology. It consists of five power switches S_1–S_5 and only one single filter inductor L_f. The PV panels and capacitor C_1 form the real dc bus while the virtual dc bus is provided by C_2 .By the switched capacitor technology, C_2 is charged by the real dc bus through S_1 and S_3 to maintain a constant voltage. This topology can be modulated with the unipolar SPWM and double-frequency SPWM. The detailed analysis is introduced as shadows.

A. Unipolar SPWM

The waveform for the unipolar SPWM of the proposed inverter is displayed in Fig. 8. The gate drive signals for the power switches are generated according to the relative value of the modulation wave *ug* and the carrier wave *uc* . Through the positive. Double-frequency SPWM for the proposed topology. Half grid cycle, *ug* >0. S1 and S3 are turned ON and S2 is turned OFF, while S4 and S5 commutate complementally with the carrier frequency. The capacitors *C*1 and *C*2 are in parallel and the circuit rotates between states 1 and 2 as shown in Fig. 10. During the

negative half cycle, *ug* <0. S5 is turned ON and S4 is turned OFF. S1 and S3 commutate with the carrier frequency circuit rotates between states 3 and 2. At state 3, S1 and S3 are turned OFF while S2 is turned ON. The negative voltage is generated by the virtual dc bus *C*2 and the inverter output is at negative voltage level. At state 2, S1 and S3 are turned ON while S2 is turned OFF. The inverter output voltage *v*AN equals zero; meanwhile, *C*2 is charged by the dc bus through S1 and S3.

B. Double -Frequency SPWM

The proposed topology can also work with double-frequency SPWM to achieve a higher equivalent switching frequency. In the double-frequency SPWM, the five power switches are separated into two parts, and are modulated with two inverse sinusoidal waves respectively. S1, S2, and S3 are modulated with *u*g1, while S4 and S5 are modulated with *u*g2. In the course of the positive half grid cycle, the circuit rotates in the sequence of "state 4 – state 1 – state 2 – state 1," and the output voltage *v*AN varies between +*V*dc and the zero with twice of the carrier frequency. During the negative half grid cycle, the circuit rotates in the sequence of "state 4 – state 3 – state 2 – state 3," and the output voltage *v*AN varies between −*V*dc and zero. The aforementioned twomodulation strategies both have their own advantages. The double-frequency SPWM can provide a higher equivalent switching frequency so that the size and weight of the filter inductor can be reduced. On the other hand, the unipolar SPWM can guarantee that the virtual dc bus *C*2 is charged by the real bus every switching cycle, so that the current stress on S1 and S3 caused by the operation of the switched capacitor can be reduced. In this paper, the unipolar SPWM is chosen as an example for the performance evaluation and experimental verification.Fig. 11. Equivalent circuits for states 2 and 3: (a) state 2; (b) state 3. For all of the four operation states, there is no limitation on the direction of the output current *i*grid, since the power switches with antiparallel diodes can achieve bidirectional current flow. Therefore, the proposed topology has the capability of feeding reactive power into the grid to help support the stability of the power system. The proposed topology is also immune against transient overvoltage of the grid. During the mains positive voltage spikes, the voltage at point A is clamped at *V*dc by *C*1 and the antiparallel diodes of S1 and S4 . Similarly, during the negative voltage spikes, the voltage at point A is clamped at −*V*dc by *C*2 and the antiparallel diodes of S2 and S5. Therefore, the mains transient overvoltage does not pose a safety threat for the inverter.

IV RECITAL EXAMINATION

In this section, the recital of the proposed circuit is analyzed in detail, including the losses distribution, the output voltage characteristics, and the CM current elimination capability. Since the H5 circuit is taken as one of the best solutions for the transformer less PV inverters, the fair performance comparison between the proposed inverter and the H5 inverter is made to explore the clear advantages of the proposed solution. The analysis is based on the unipolar SPWM and unit output power factor.

A. Conduction Losses in the Power Devices

During the positive half cycle, the proposed inverter works just like the unipolar modulated full-bridge inverter. At state 1, the output current *i*grid flows through S1 and S4 ; at state 2, *i*grid flows through S3 and S5 . There are always two switches on the path of *i*grid. During the negative half cycle, however, the situation is different. On one hand, there are still two switches on the path of *i*grid. On the other hand, the charging of the switched capacitor *C*2 gives rise to some extra current on S1 and S3. This charging current causes some extra conduction losses.

B. Conduction Losses in Switched Capacitors

The operation of the switched capacitor also increases the conduction losses in the capacitor due to its equivalent series resistance (ESR). The ESR losses are evaluated to give further guidelines on the capacitor design. For the proposed topology, the conduction losses in ESR can be divided into two parts. The major part is caused by the ripple current which is inherent to all voltage source inverters, including the traditional full-bridge and half-bridge circuits and the newly developed topologies such as H5, HERIC, etc. The second part is caused by the inrush current during the charging of the switched capacitors.

C. Switching Losses

During the positive half cycle, only two switches, namely S4 and S5, commutate at the carrier frequency, so the switching losses are the same as the traditional full-bridge inverter. During the negative half cycle, S1, S2, and S3 commutate at the carrier frequency. Although the number of high-frequency switches increases to 3, it can be seen from the following analysis that the switching losses almost keep the same. For convenience of description, the power transistor and the antiparallel diode for the switch S*n* is denoted as T*n* and D*n* respectively, where *n* = 1, 2, 5. At state 2, T1, T3 , and T5 are turned ON, while the current actually flows through T1, D3 , and T5. When the circuit switches from state 2 to state 3, T1 and T3 are turned OFF first before T2 is turned ON due to the effect of the dead time. As a result, there will be a transition state between the two states. During this transition state, the inductor *Lf* freewheels through D3, so the voltage across T1 and T3 may not rise immediately after turned OFF, so that the switching losses can be neglected. When the dead time is passed, T2 is turned ON. The inductor current is forced to commutate from D3 to T2 , and the circuit changes into state 3. When the circuit rotates from state 3 to state 2, it also enters the transition state first. Because of the dead time, T2 is turned OFF while T1 and T3 are not turned ON yet, and the inductor current is forced to commutate from T2 to D3. After D3 is conducting, the voltage across S1 and S3 reduces to zero approximately. Therefore, when T1 and T3 are turned ON after the transition state, they will not suffer significant switching losses.

D. Losses in the Filter Inductor

Further down the same switching frequency, the output voltage waveforms of the proposed circuit and the H5 circuit are identical to each other. This results in similar output current ripple and magnetic losses, if the same filter inductor configurations are used. On the other hand the H5 circuit has to employ two inductors with separated iron cores, while the proposed circuit only needs one. This might lead to a reduction in the size of the iron core, although the total inductor value is still the same.

E. CM Current Elimination

As explained formerly the key point for the full-bridge based solutions, including H5 and HERIC, is to insert extra switches into the traditional full-bridge inverter to disconnect the line side with the dc side once the inverter output voltage is at zero voltage level. Inappropriately this disconnection is incomplete because of the parasitic capacitance on the power switches. As a result, high-frequency CM current may still flow through these capacitors. Therefore, it is essential to add extra filters into these topologies to absorb this CM current [21]–[23].
As for the proposed topology, the stray capacitance between the PV panels and the ground is directly bypassed. Due to the configuration of the virtual dc bus, the CM current is eliminated completely.

V CONCLUSION

The concept of dc – dc converter and virtual dc bus in photovoltaic inverter, 1, Which provide constant supply to the inverter in varying environment due to climatic barrier and prevent the cause of damage to load due to this variations 2, CM leakage current eliminated completely by connecting PV negative terminal to the grid neutral point which also help to generate negative half cycle switching is triggered and control by PIC Microcontroller. 3, Due to the bi-directional nature of the proposed circuit reactive power is reduced which increases the efficiency of the inverter in commercial purpose.

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