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RESEARCH ARTICLE

IMPLEMENTATION OF HARDWARE IP ROUTER BASED ON VLSI

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Abstract: Through this paper our attempt is to give a onetime networking solution by the means of merging the VLSI field with the networking field as now a days the router is the key player in networking domain so the focus remains on that itself to get a good control over the network, Networking router today are with minimum pins and to enhance the network we go for the bridging loops which effect the latency and security concerns. The other is of multiple protocols being used in the industry today. Through this paper the attempt is to overcome the security and latency issues with protocol switching technique embedded in the router engine itself. This paper is based on the hardware coding which will give a great impact on the latency issue as the hardware itself will be designed according to the need. In this paper our attempt is to provide a multipurpose networking router by means of Verilog code, by this we can maintain the same switching speed with more secured way of approach we have even the packet storage buffer on chip being generated by code in our design in the so we call this as the self-independent router called as the VLSI Based router. This paper has the main focus on the implementation of hardware IP router. The approach here is that router will process multiple incoming IP packets with different versions of protocols simultaneously and even it is going to hold true for the IPv4 as well as for IPv6. With the approach of increasing switching speed of a routing per packet for both the current trend protocols. This paper thus is going to be a revolutionary enhancement in the domain of networking.

Keywords: IPv4; VLSI; VLSI Based router

Full Text: <http://www.ijcsmc.com/docs/papers/December2013/V2I12201364.pdf>