



A Modified Three-Phase-Four-Wire UPQC with Minimum VA Rating for Power Quality Improvement

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Abstract— *The unified power quality conditioner (UPQC) is a custom power device, which mitigates voltage and current-related PQ issues in the power distribution systems. In this paper, a UPQC topology for applications with non-stiff source is proposed. The proposed topology enables UPQC to have minimum VA rating without compromising its compensation capability. This proposed topology also helps to match the dc-link voltage requirement of the shunt and series active filters of the UPQC. The topology uses a capacitor in series with the interfacing inductor of the shunt active filter, and the system neutral is connected to the negative terminal of the dc-link voltage to avoid the requirement of the fourth leg in the voltage source inverter (VSI) of the shunt active filter. The average switching frequency of the switches in the VSI also reduces, consequently the switching losses in the inverters reduce. Detailed design aspects of the series capacitor and VSI parameters have been discussed in the paper. In this proposed method the total power handled by modified UPQC is minimum than the other conventional methods and it has been investigated by simulation using MATLAB/SIMULINK.*

Keywords- Average switching frequency, minimum VA rating, hybrid topology, non-stiff source, unified power quality conditioner (UPQC).

1. Introduction

With the advancement of power electronics and digital control technology, the renewable energy sources are increasingly being connected to the distribution systems. On the other hand, with the proliferation of the power electronics devices, nonlinear loads and unbalanced loads have degraded the power quality (PQ) in the power distribution network [1]. Custom power devices have been proposed for enhancing the quality and reliability of electrical power. Unified PQ conditioner (UPQC) is a versatile custom power device which consists of two inverters connected back-to-back and deals with both load current and supply voltage imperfections. UPQC can simultaneously act as shunt and series active power filters. The series part of the UPQC is known as dynamic voltage restorer (DVR). It is used to maintain balanced, distortion free nominal voltage at the load. The shunt part of the UPQC is known as to compensate load reactive power, harmonics and balance the load currents thereby making the source current balanced and distortion free with unity power factor.

UPQC is a modern CUSTOM power device[9]-[11], which is used to solve almost all types of power quality problems. The UPQC consists of series and shunt active filter as shown in fig.1. Series active filter is used to mitigate the voltage sag and swell problems and shunt active filter is used to improve the power factor and eliminate the load harmonics. In series active filter the voltage will be injected at an optimum angle. In that optimum angle total VA requirement of UPQC will be less than the UPQC-P (series injected voltage is in phase with the source current) and the UPQC-Q (series injected voltage is in

900 with the source current) method. Therefore, the active power requirement will be less than the UPQC-P and an injected voltage magnitude is less than the UPQC-Q. The minimum VA method is one of the effective methods among others.

In case of the three-phase four-wire system, neutral-clamped topology is used for UPQC [25], [26]. This topology enables the independent control of each leg of both the shunt and series inverters, but it requires capacitor voltage balancing [27]. In [21], four-leg VSI topology for shunt active filter has been proposed for three-phase four-wire system. This topology avoids the voltage balancing of the capacitor, but the independent control of the inverter legs is not possible. To overcome the problems associated with the four-leg topology, in [28], [29], the authors proposed a T-connected transformer and three-phase VSC based DSTATCOM. However, this topology increases the cost and bulkiness of the UPQC because of the presence of extra transformer.

In this paper, a UPQC topology with minimum VA rating is proposed. The topology consists of capacitor in series with the interfacing inductor of the shunt active filter. The series capacitor enables reduction in dc-link voltage requirement of the shunt active filter and simultaneously compensating the reactive power required by the load, so as to maintain unity power factor, without compromising its performance. This allows us to match the dc-link voltage requirements of the series and shunt active filters with a common dc-link capacitor. Further, in this topology, the system neutral is connected to the negative terminal of the dc bus. This will avoid the requirement of the fourth leg in VSI of the shunt active filter and enables independent control of each leg of the shunt VSI with single dc capacitor. The simulation studies are carried out using MATLAB/Simulink software, and detailed results are presented in the paper. A prototype of three-phase UPQC is developed in the laboratory to verify the proposed concept, and the detailed results are presented in this paper.

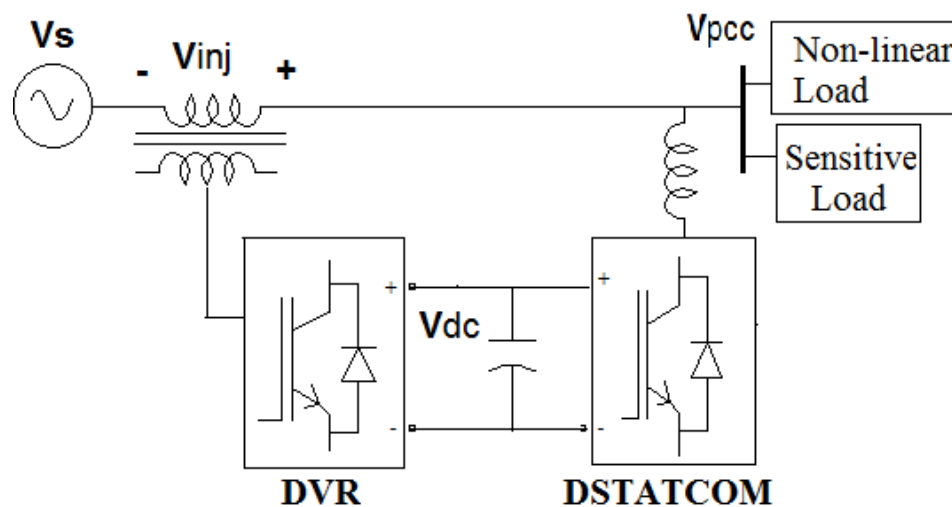


Figure.1. Schematic diagram of UPQC

2. EXISTED UPQC WITH MINIMUM VA

In this minimum VA method the voltage injection will be based on an optimum angle α . α is an angle between the post sag source voltage and the load voltage shown in figure.4. Optimum angle is an angle in which the VA requirement of the UPQC will be minimum[5]. Based on this optimum angle, the magnitude of injected voltage and the injection angle will be derived. In that particular magnitude of injected voltage and an injection angle, the active power requirement of the UPQC will be less than the UPQC-P method and the reactive power requirement of the UPQC will be less than the UPQC-Q method. So the total VA requirement of the UPQC will be less compare to the other two methods. And also the magnitude of injected voltage will be less than the UPQC-Q method. So the minimum VA method is one of the very efficient method. The injected voltage and the power limitation in the minimum VA method (V, P, Q and S indicates injected voltage, real, reactive and apparent power and subscripts such as $In, Quad, Min$ indicates UPQC-P, UPQC-Q, Minimum VA method) will be,

$$\begin{aligned}
 V_{In} &< V_{Min} < V_{Quad} \\
 P_{Quad} &< P_{Min} < P_{In} \\
 Q_{In} &< Q_{Min} < Q_{Quad} \\
 S_{Min} &< S_{In} < S_{Quad}
 \end{aligned}$$

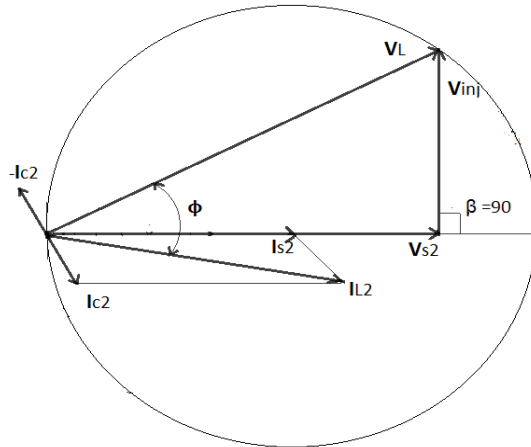


Figure.2. Phasor diagram of Quadrature compensation method

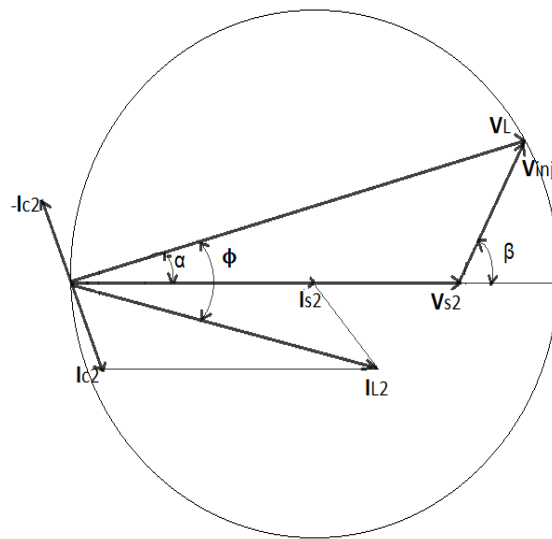


Figure.3. Phasor diagram of Minimum VA method

3. PROPOSED UPQC TOPOLOGY WITH MINIMUM VA RATING

Fig. 4 represents the equivalent circuit of the proposed VSI topology for UPQC compensated system. In this topology, the system neutral has been connected to the negative terminal of the dc bus along with the capacitor C_f in series with the interfacing inductance of the shunt active filter. This topology is referred to as modified topology.

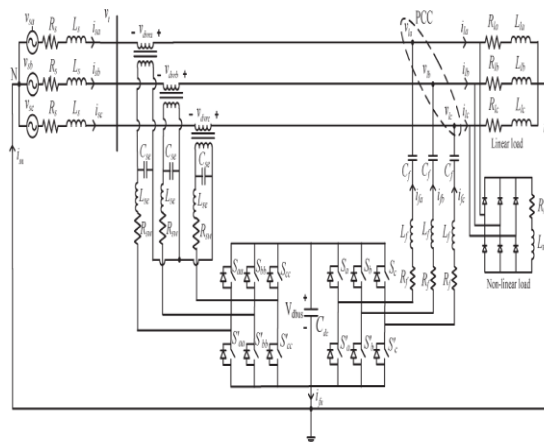


Figure.4. Equivalent circuit of proposed VSI topology for UPQC compensated system (modified topology).

A. Minimum VA Calculation

The total VA requirement of the UPQC (*SUpqc*) from fig.5. is depending on the VA requirement of both the series(*SSr*) and shunt active filter(*SSh*) [5]. By considering the presag source voltage and the postsag load voltage (*VL*) are 1 p.u, we can write the total VA requirement is in terms of the load displacement power factor ($\cos\phi$), the sag in p.u, and an optimum angle. Here, *Rs*, *Ls* is series resistance and inductance respectively.

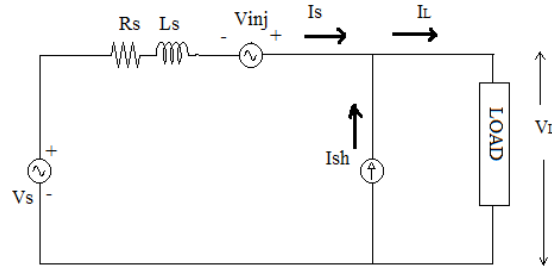


Figure.5. Equivalent circuit of UPQC

$$S_{upqc} = S_{sr} + S_{sh} \quad (I)$$

In this case we are taking the load current as constant in both the normal and the sag condition. So the load current is considered as 1 p.u.

B. Minimum VA Algorithm

- Step (1): Initialize $\alpha=0$ and $TVA1=100$
- Step (2): Get input values of sag and p.f. angle
- Step (3): Check $\alpha \leq \text{p.f. angle}$,
if it is true go to step(4),
if it is false go to step(7)
- Step (4): find the value of new TVA
- Step (5): Check $TVA1 < TVA$
- Step(6): If (5) is false, assume $TVA1=TVA$, and then increase the α by 1 and go to step(3). If (5) is true go to step(7)
- Step(7): find the values of V_{inj} and β for corresponding optimum angle $\alpha-1$ and print the result.

4. DESIGN OF VSI PARAMETERS FOR PROPOSED TOPOLOGY

The parameters of the VSI need to be designed carefully for better tracking performance. The important parameters that need to be taken into consideration while designing conventional VSI are V_{dc} , C_{dc} , L_f , L_{se} , C_{se} , and switching frequency (f_{sw}). The design details of the VSI parameters for the shunt and series active filter are given in [31], [32]. Based on the following equations, the parameters of the VSIs are chosen for study.

A. Design of Shunt Active Filter VSI Parameters

Consider the active filter is connected to an X kVA system and deals with 0.5X kVA and 2X kVA handling capability under transient conditions for n cycles. During transient, with an increase in system kVA load, the voltage across each dc-link capacitor (V_{dc}) decreases and vice versa. Allowing a maximum of 25% variation in V_{dc} during transient, the differential energy (ΔE_c) across C_{dc} is given by

$$\Delta E_c = \frac{C_{dc} [(1.125V_{dc})^2 - (0.875V_{dc})^2]}{2} \quad (1)$$

The change in system energy (ΔE_s) for a load change from 2X kVA to 0.5X kVA is

$$\Delta E_s = (2X - X/2)nT \quad (2)$$

Equating (1) and (2), the dc-link capacitor value is given by

$$C_{dc} = \frac{2(2X - X/2)nT}{(1.125V_{dc})^2 - (0.875V_{dc})^2} \quad (3)$$

where, V_m is the peak value of the source voltage, X is the kVA rating of the system, n is number of cycles, and T time period of each cycle. An empirical study has been carried out for various values of interfacing inductance values with the variation of the dc-link voltage in [31], with $V_{dc} = mV_m$, and it is found that $m = 1.6$ gives fairly good switching performance of the VSI. The approximate relationship between m and minimum (f_{swmin}), maximum switching frequency (f_{swmax}) is obtained by analysis of the VSI in [31], and this is given below. For switching frequency variation approximately from 6 kHz to 10 kHz, the value of m is 1.58, which is taken as 1.6 in the study

$$m = \frac{1}{\sqrt{1 - f_{swmin}/f_{swmax}}} \quad (4)$$

Based on this, the shunt interfacing inductance has been derived taking into consideration of the maximum switching frequency and is given below [31]

$$L_f = \frac{mV_m}{4h_1 f_{swmax}} \quad (5)$$

Where

$$h_1 = \sqrt{\frac{k_1}{k_2} \frac{(2m^2 - 1)}{4m^2} f_{swmax}} \quad (6)$$

where, h_1 is the hysteresis band limit, k_1 and k_2 are proportionality constants.

B. Design of Series Active Filter VSI Parameters

In order to make the series active filter system a first-order system, a resistor is added in series with the filter capacitor, referred as switching band resistor (R_{sw}) [32].

The rms value of the capacitor current can be expressed as $I_{se} = \sqrt{I_{inv}^2 - I_l^2}$. I_{inv} is the series inverter current rating and I_l is the load current. The capacitor branch current is divided into two components—a fundamental current I_{se1} , corresponding to the fundamental reference voltage (V_{ref1}) and a switching frequency current I_{sw} , corresponding to the band voltage (V_{sw}).

The DVR voltage and the current of the capacitor are given by

$$\begin{aligned} V_{dvr} &= \sqrt{V_{ref1}^2 + V_{sw}^2} \\ I_{se} &= \sqrt{I_{se1}^2 + I_{sw}^2} \\ V_{sw} &= I_{sw} R_{sw} = \frac{h_2}{\sqrt{3}} \\ V_{ref1} &= I_{se1} X_{se1} = \frac{I_{se1}}{2\pi f_1 C_{se}} \end{aligned} \quad (7)$$

where h_2 is the hysteresis band voltage. The resistance (R_{sw}) and the capacitance (C_{se}) values are expressed in terms of band voltage v_{sw} and rated references voltage (V_{ref1}), respectively, and are given by

$$\begin{aligned} R_{sw} &= \frac{h_2}{I_{sw} \sqrt{3}} \\ C_{se} &= \frac{I_{se1}}{V_{ref1} 2\pi f_1} \end{aligned} \quad (8)$$

The interfacing inductor L_{se} has been designed based on the switching frequency of the series active filter and is given by

$$L_{se} = \frac{(V_{bus}) R_{sw}}{4 f_{swmax} h_2} \quad (9)$$

where V_{bus} is the total dc-link voltage across both the dc-link capacitors.

C. Control Circuit

The control circuitry for both the topologies is same and is shown in Fig. 3. Only six switching commands are to be generated. These six signals along with the complementary signals will control all the 12 switches of the two inverters.

The switching control law for shunt active filter is given as follows.

If $i_{fa} \geq i_{fa}^* + h1$, then bottom switch is turned ON whereas

top switch is turned OFF ($S_a = 0, S'_a = 1$).

If $i_{fa} \leq i_{fa}^* - h1$, then top switch is turned ON whereas bottom switch is turned OFF ($S_a = 1, S'_a = 0$).

Similarly the switching commands for series active filter is given as follows.

If $vdvra \geq v_{dvra}^* + h2$, then bottom switch is turned ON whereas top switch is turned OFF ($S_{aa} = 0, S'_{aa} = 1$). If $vdvra \leq v_{dvra}^* - h2$, then top switch is turned ON whereas bottom switch is turned OFF ($S_{aa} = 1, S'_{aa} = 0$).

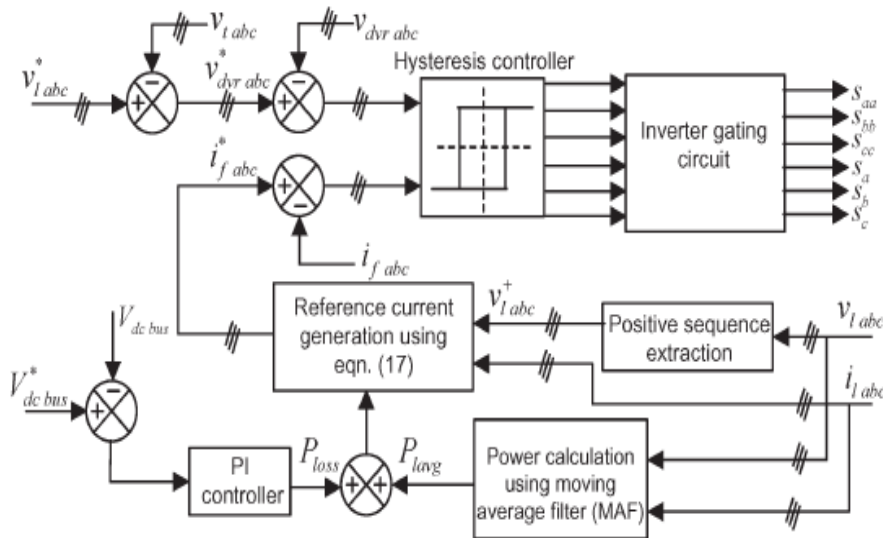


Figure.6. Control Circuit for Series and Shunt Converters of UPQC

4. SIMULATION RESULTS

A. Existed System

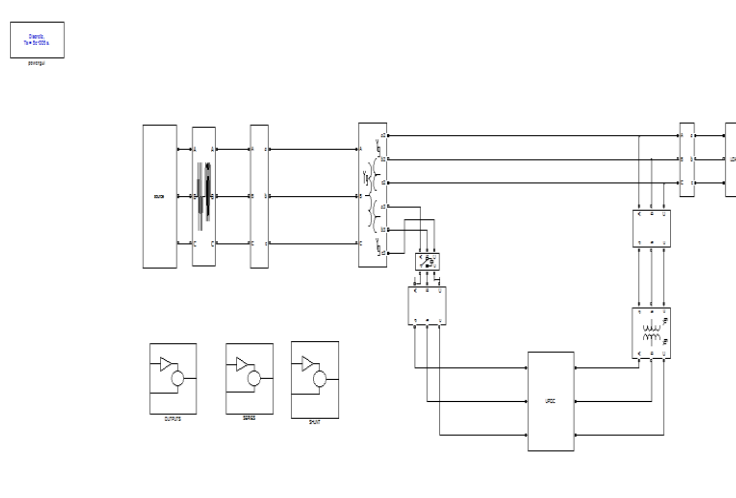


Figure.7. Simulation of Existed System

B. Proposed System

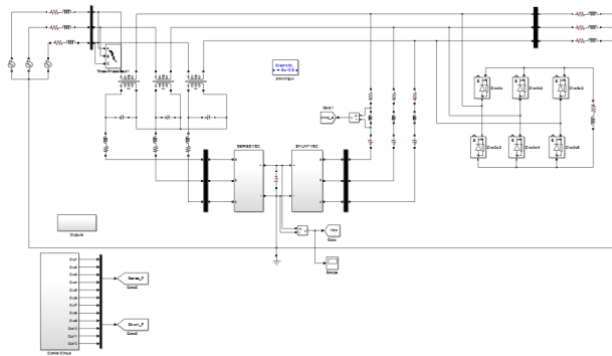


Figure.12. Simulation Circuit with Proposed Automation Control Strategy

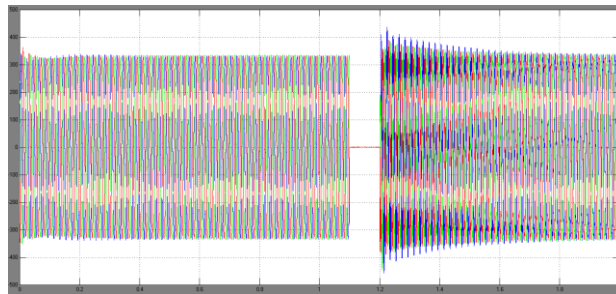


Figure.13. Source Voltages

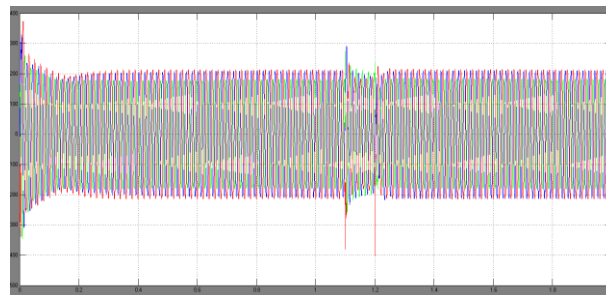


Figure.14. Load Voltages

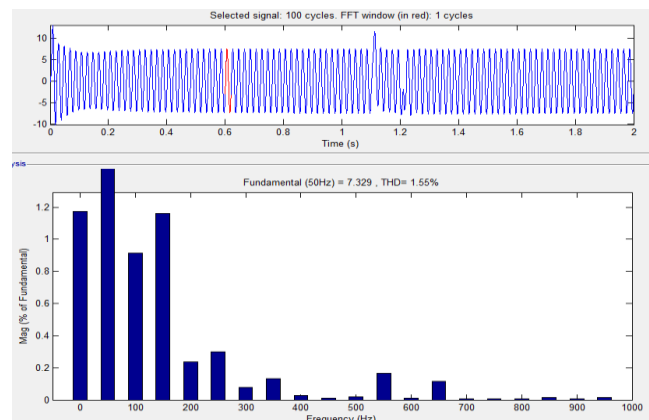


Figure.15. THD Spectrum of Source Currents

5. CONCLUSION

In this paper the sag of the load voltage has been compensated by using the modified three phase four wire UPQC with minimum VA loading. And the total harmonic distortion of the source current has been reduced with the improved power factor. The results of sag compensation with the existed topology are obtained separately and that results are compared with the proposed topology. Though the configuration of UPQC is modified it is still maintaining the minimum VA rating. The THD is low in the proposed system. And also the active power handled by the UPQC is less than the UPQC-P and the injected voltage through the series active filter is less than the UPQC-Q.

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