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A Literature Survey on Low PDP Adder Circuits

PUNITHA S, MANOHARAN K

Assistant Professor, Department of Electronics and Communication Engineering, SVS College of Engineering, Coimbatore, India

Abstract: *In this paper, the various low power full adder circuits with high speed operation have been analyzed. The adder is the basic building blocks of arithmetic circuits, so a small amount of power or delay reduction leads to greatest power saving or better performance of the circuit. Various design techniques are available for low power high speed full adders. All the adders are simulated using tanner EDA tools with 45nm technology. The power consumption and delay of various adders have been computed and analyzed. Also power delay product and number of transistors for each design has been calculated and compared with other design. These performance results will help the circuit designer to choose right adder for their required application.*

Keywords: *Low power, Full Adder, Low Power delay products, Very Large Scale Integration Circuits.*

1. INTRODUCTION

Nowadays designing a low power, high speed VLSI system is more important for fast growing portable devices. The power consumption is the most important issue while designing high speed portable devices. The power consumption and speed are the major conflicting design aspects in low power VLSI design; hence Power Delay Product (PDP) is used to analyze its circuit performance. Adder is one of the speed limiting elements in integrated circuits. The full adder is used for performing arithmetic operations such as addition, subtraction, multiplication and division. The power consumption of full adder has to be reduced so that overall all power consumption of the chip is reduced. The propagation delay can be optimized to get high speed operation. The adder modules have been briefly discussed in the following section.

2. TYPES OF FULL ADDERS

2.1 Conventional CMOS Full Adder

The most basic full adder is conventional CMOS and contains 28 transistors [1]. It contains PMOS transistors in pull-up network and NMOS transistors in pull-down network. A, B and C_{in} are the inputs and Sum & C_{out} are the outputs. The main advantages of the conventional CMOS full adder are its most stable operation and robust performance. The drawback of this adder is high Sub-threshold leakage level. The Conventional CMOS Full Adder is shown in Figure 1.

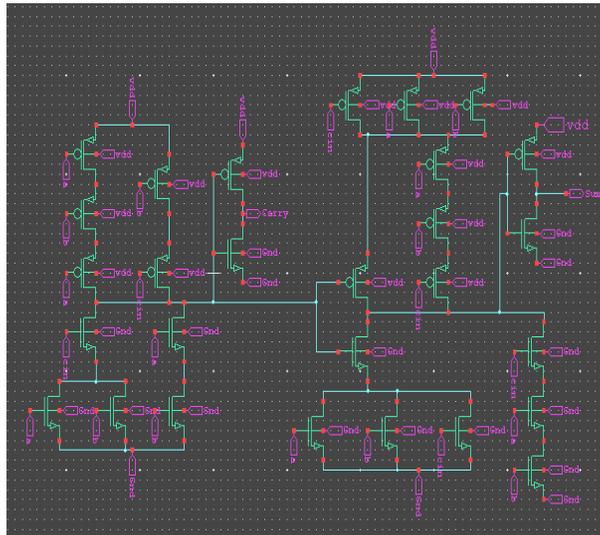


Figure 1: Conventional CMOS Full adder

2.2 Transmission Function Full Adder (TFA)

Transmission function full adder [2] is one types of full adder and it contains 16 transistors. The inputs are ‘a’, ‘b’ and ‘c’ and the outputs are sum and carry. Both NMOS and PMOS transistors are used. This adder has no problem of voltage drop. The main advantage is low power consumption [3]. Lack of driver capability and requires more number of transistors are the main disadvantages.

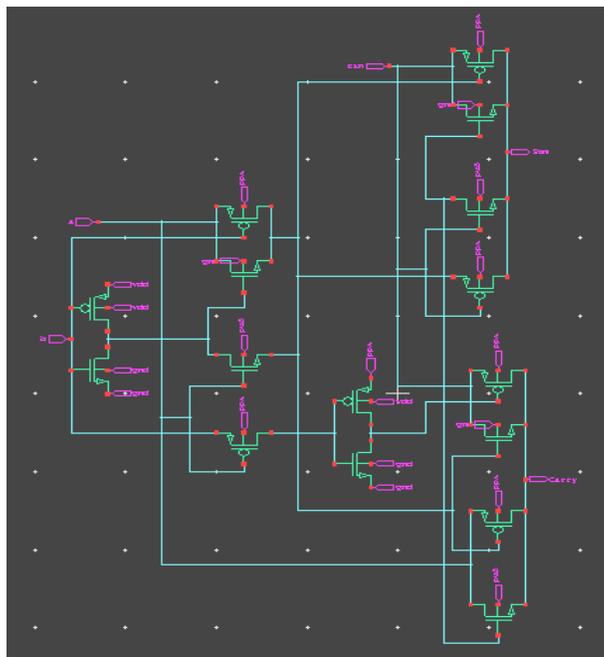


Figure 2: Transmission Function full adder (TFA)

2.3 10T Full Adder

10T full adder [3] consists of 10 transistors. A, B and C_{in} are the inputs and sum and carry are the outputs. It requires two XOR operations to calculate the sum function. Each XOR operation requires 4T transistors. 2X1 MUX is used for carry function and implemented using two transistors. First, it generates A XOR B and it is used to generate the output along with its complement of select signal. This adder cannot work under 0.5V. Due to its supply voltage, the delay is small. The only disadvantage is high capacitance value produced for their inputs. Loading the inputs in this adder is slow.

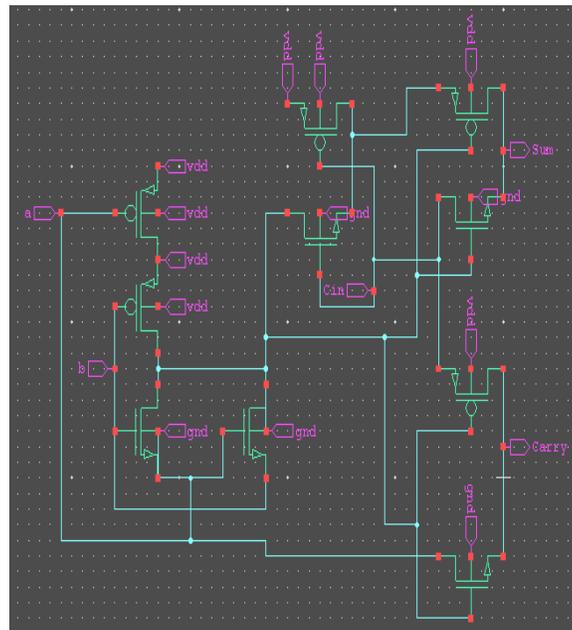


Figure 3: 10T Full adder

2.4 Transmission Gate Full Adder (TGA)

Transmission gate full adder [4] is based on transmission gate logic and it consists of 20 transistors. The PMOS and NMOS transistors are connected in parallel manner. The inputs are a, b and c and the outputs sum and carry. No voltage drop arises is the main advantage in this adder. It can be used to design XOR and XNOR gates because it consumes low power. The number of transistors needed is twice to design the TGA.

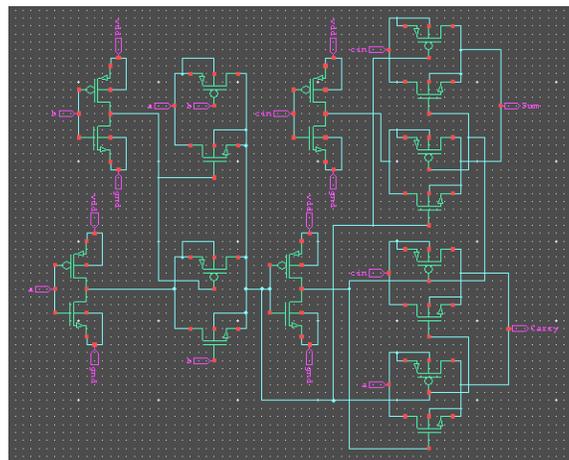


Figure 4: Transmission gate full adder (TGA)

2.5 14T Full Adder[5]

The adder consists of 14 transistors. The inputs are A, B and C_{in} and the outputs are sum and carry. The pass transistor logic is used to generate sum and transmission gate logic is used to generate carry.

It produces the better result in threshold loss, speed and power by sacrificing four extra transistors per adder cell. Even though the transistor count increases by four per adder cell, it reduces the threshold loss problem. Better cascading capability, low power consumption and higher operating frequency are the advantages in 14T.

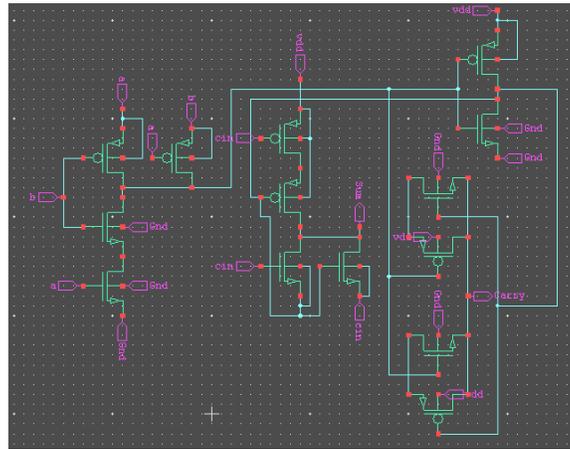


Figure 5: 14T full adder

2.6 Static Energy Recovery Full Adder (SERF)

Static energy recovery full adder [6] consists of 10 transistors. The inputs are A, B and C_{in} and the outputs are sum and carry. The power consumption is reduced by using energy recovery technique. This adder operates well at higher voltages and this circuit fails to work when the voltage lower than 0.3 V. In new SERF adder, there is no direct path to the ground. The SERF full adder is the energy recovery technique because of the combination of not having a direct path to ground and the re-application of the load charge to the control gate. This adder does not provide full swing and it cannot be cascaded at low power supply. This adder cannot work correctly at low voltages and high delay is occurred.

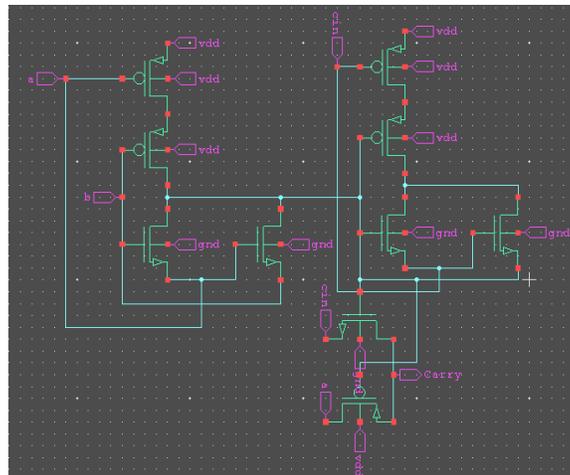


Figure 6: Static Energy Recovery Full adder (SERF)

2.7 Gate Diffusion Input Full Adder (GDI)[7]

Gate diffusion input is a technique for low power digital circuit design in an embedded system. It has 10 transistors and it has three inputs namely G (gate input to NMOS/PMOS), N (input to source of NMOS) and P (input to source of PMOS). It is the high performance and low power full adder. High to low transition characteristics of PMOS pass transistor is poor so that low swing occurred for the input combination 00. The main problem of a GDI cell is that it needs twin-well CMOS or silicon on insulator (SOI) process to realize.

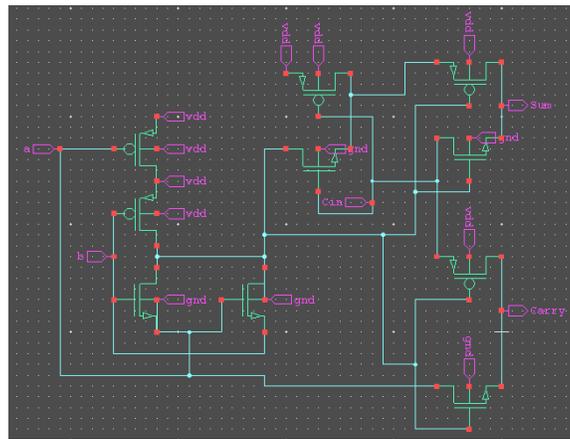


Figure 7: Gate Diffusion Input full adder (GDI)

2.8 Complementary Pass-Transistor Full Adder (CPL)

Complementary pass transistor full adder [1] is based on NMOS pass transistor logic and it contains 32 transistors. In this adder, low input capacitance, high speed operation and threshold voltage loss in the output circuit are achieved. It also consumes low power and reduces noise margin.

The main advantage is that it has good driving capability due to output inverters and small input capacitance. It requires two MOS networks and cascading particularly in low voltages are the major problems.

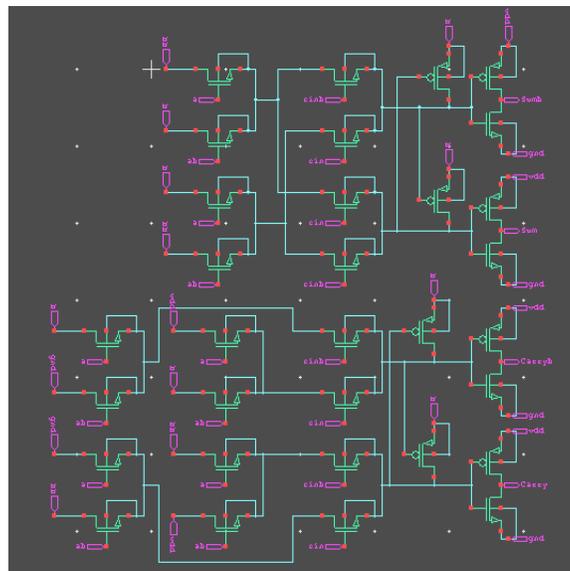


Figure 8: Complementary Pass – Transistor full adder (CPL)

2.9 8T Full Adder[8]

This adder consists of 3T XOR gates and contains 8 transistors. Thus, it is the low-cost and low-area cell. It consists of 3 modules namely 2 XOR elements and a carry section. The Sum and the Carry module need 6 and 2 transistors respectively. Due to minimum number of transistors, this adder works at high speed with low power dissipation and the small transistor delay. No threshold voltage loss is occurred. The main disadvantage is that three input capacitances are used to implement different functions.

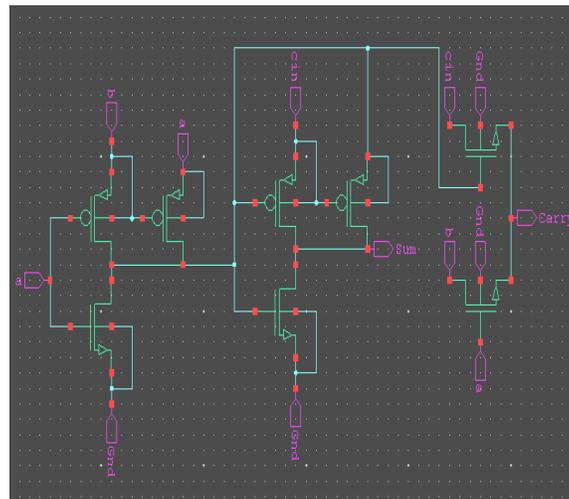


Figure 9: 8T Full adder

2.10 Multiplexer Based Full Adder (MB12T)[9]

This adder has 12 transistors and 6 multiplexers. The pass transistor logic with two transistors technique is used for implementing each multiplexer. In this full adder circuit, it has no VDD and GND connection. Thus, short circuit power can be decreased. High delay is achieved for producing sum signal due to high fan out and the area of the adder circuit is increased.

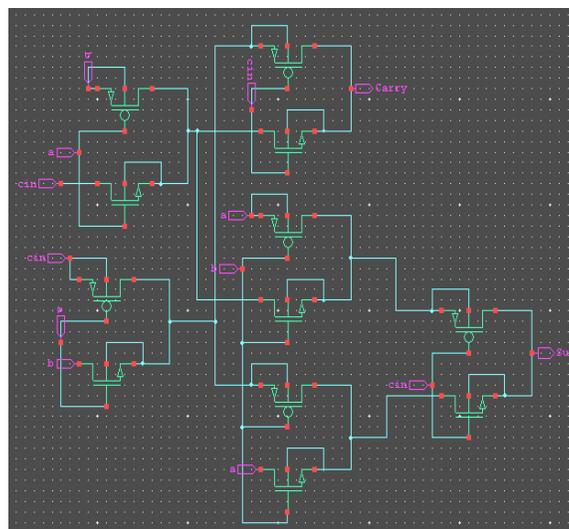


Figure 10: Multiplexer based full adder (MB12T)

2.11 Complementary and Level Restoring Carry Logic Full Adder (CLRCL)[10]

This adder has 10 transistors and consists of 2x1 MUX and CMOS inverters to implement sum and carry functions. No threshold loss occurred in this adder.

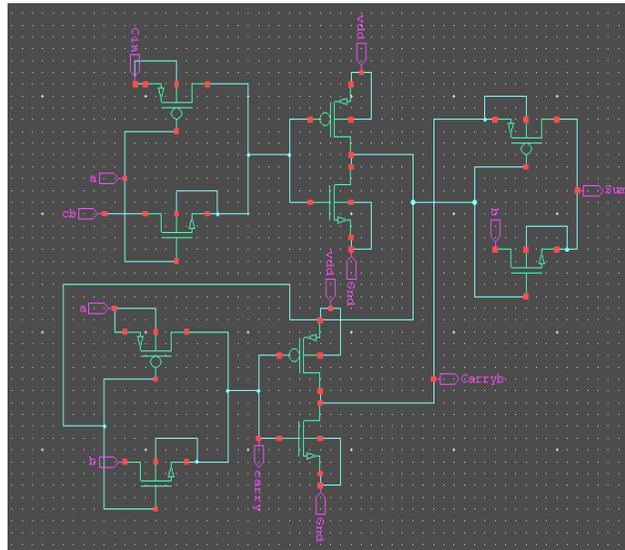


Figure 11: Complementary and Level Restoring Carry Logic Full Adder (CLRCL)

3. COMPARISON OF DIFFERENT FULL ADDERS

Table 1: Comparison of different full adders

Design	Power (μ W)	Delay (ns)	PDP (aj)	No. of transistors
CMOS	0.95	143.13	135.68	28
TFA	1.05	141.92	148.37	18
10T	0.27	1431.08	390.15	10
TGA	1.07	144.08	153.88	20
14T	0.67	792.41	529.17	14
SERF	1.74	401.05	695.88	10
GDI	0.34	286.31	96.93	10
CPL	1.36	138.70	189.31	32
8T	0.42	178.48	74.77	8
MB12T	0.37	252.35	94.38	12
CLRCL	0.52	213.56	111.27	10

3.1 Power Comparison

SERF dissipates more power compared to other adders. Due to dual-rail structure and higher number of nodes, CPL wastes more power. The short circuit power and switching power is increased in TGA and TFA. CLRCL dissipates less power compared to SERF, CPL, TGA and TFA. 8T dissipates less power due to its transistors count. The power dissipation is low in 14T. GDI and MB12T dissipates less power. 10T dissipates much low power compared to all adders. Figure 12 shows different types of adder vs. power consumption.

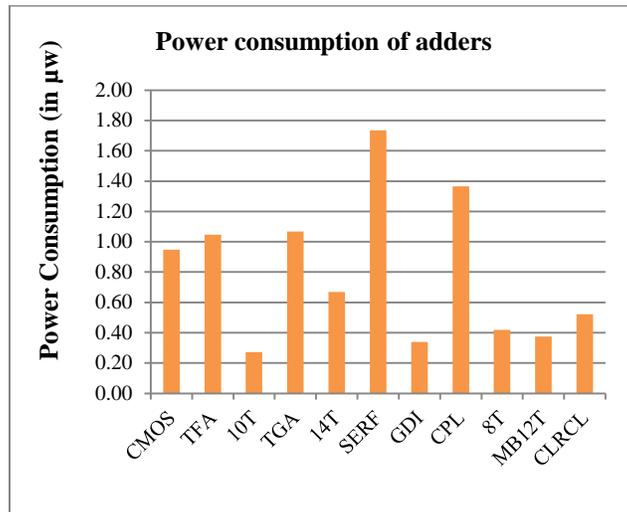


Figure 12: Different types of adder vs. Power consumption

3.2 Delay Comparison

The 8T full adder delay is slower than CLRCL adder. CMOS, TFA and TGA produces almost nominal and same delay compared to GDI, MB12T and CLRCL. CPL produces negligible delay compared to all other adders.

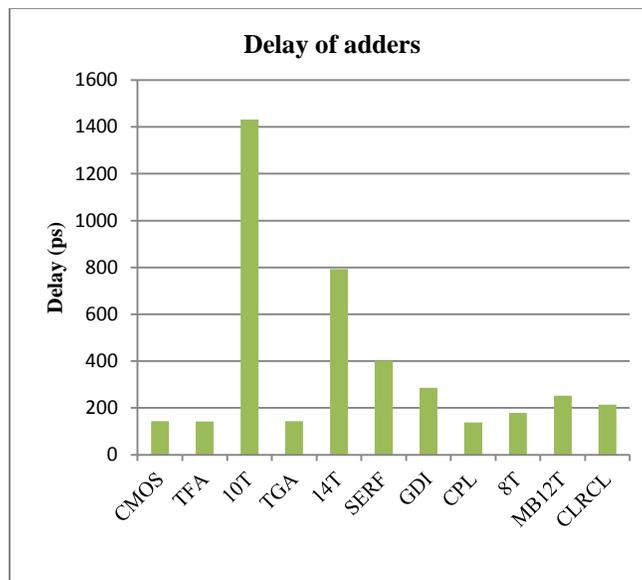


Figure 13: Different types of adders vs. Delay

3.3 PDP Comparison

The Power Delay Product (PDP) increases by increasing power consumption and time delay. SERF, 14T and 10T produce higher PDP than conventional CMOS adder. The CMOS, TFA, TGA, CPL, MB12T and CLRCL have lower PDP and gives almost similar results. The best PDP is 8T compared to all others. The figure14 shows adders versus PDP.

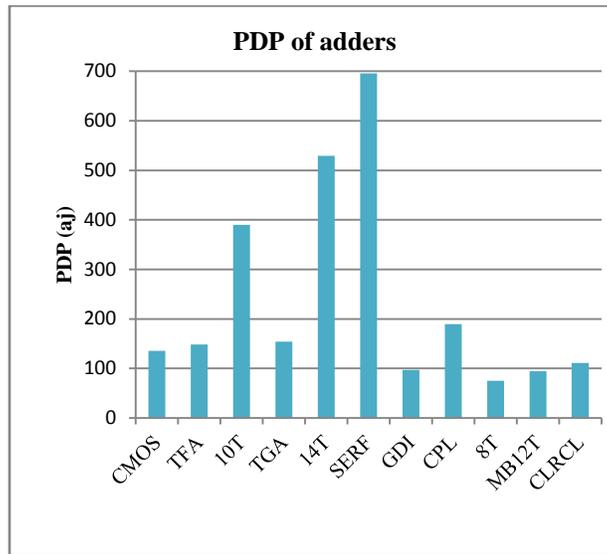


Figure 14: Different types of adders vs. PDP

3.4 Transistor Comparison

Conventional CMOS and CPL uses more number of transistors. TFA uses more transistors compared to 14T and MB12T and lower than CMOS and CPL. 10T, SERF, GDI and CLRCL use 10 transistors. 8T is the least number of transistors used compared to all other adders.

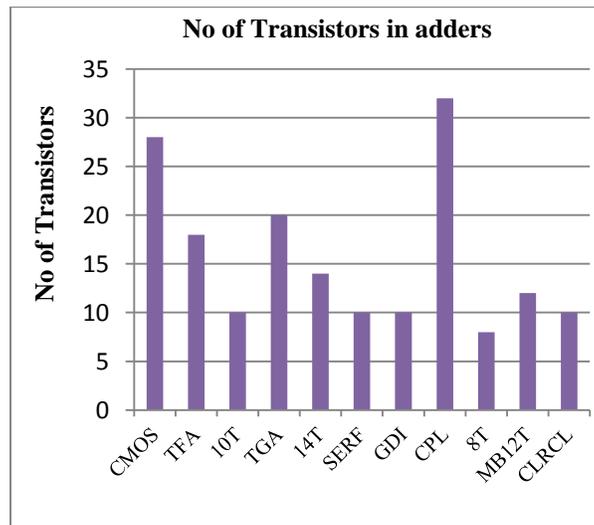


Figure 15: Different types of adders vs. No. of transistors

4. CONCLUSION

Thus the different types of full adders have been studied and comparison of different full adders in terms of power, delay, PDP and no. of transistors is done. Based on this comparison, 8T full adder is the best power consuming adder and it consumes less delay and PDP. The transistor count is also very low compared to all other adders. This adder is suitable for VLSI applications with very low power consumption and delay. Due to reduction in number of transistors, switching activity is reduced. The short circuit current is eliminated by its dynamic characteristics.

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