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# LOW POWER BARREL SHIFTER DESIGN USING COMPLEMENTARY AND PSEUDO NMOS LOGIC

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**Abstract**— *the purpose of the paper is to design the barrel shifter using complementary logic and pseudo dynamic logic. The barrel shifter is essential segment in ALU. The 2:1 mux design using static cmos or pseudo nmos logic is used for the shifting operation in left direction or in right direction. The design of barrel shifter and simulations are done on CADENCE Virtuoso 6.1 tool. The methodology in this work are (1) CMOS static logic (2) Pseudo NMOS logic. This work evaluates on 180nm technology. It is design to reduce area, delay and power of barrel shifter in ALU. At the end, both the logic structures are analyzed and optimize area logic is purposed.*

**Index Terms**— *Barrel shifter, CADENCE Virtuoso 6.1, Static CMOS logic, Pseudo NMOS logic, 180nm*

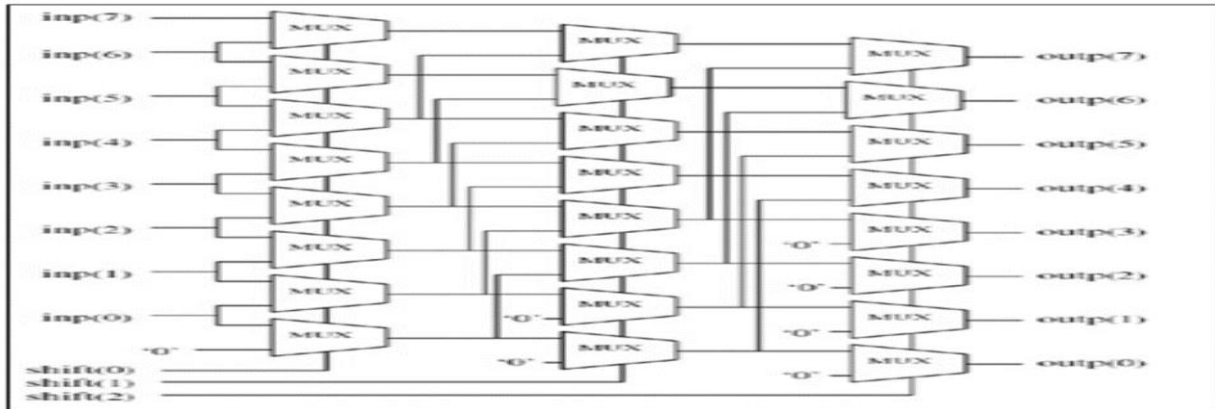
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## I. INTRODUCTION

Barrel shifter is essential components in ALU. Barrel shifter is often used for shifting operation like shift right logical, shift left logical, shift left arithmetic, shift right arithmetic, right rotate, left rotate. The architecture of barrel shifter can be designed by using 2:1, 4:1, 8:1, 16:1 Mux trees. Barrel shifter is most essential element in DSP applications. Barrel shifter is designed using Mux trees to use it in repetitive form so that power consumed by the barrel shifter should minimum.

## II. BARREL SHIFTER

Barrel shifter is combinational logic circuit with ‘n’ number of data inputs and data outputs and set of control inputs which are used to perform shifting operation.



**Fig.1. Block diagram of Barrel shifter**

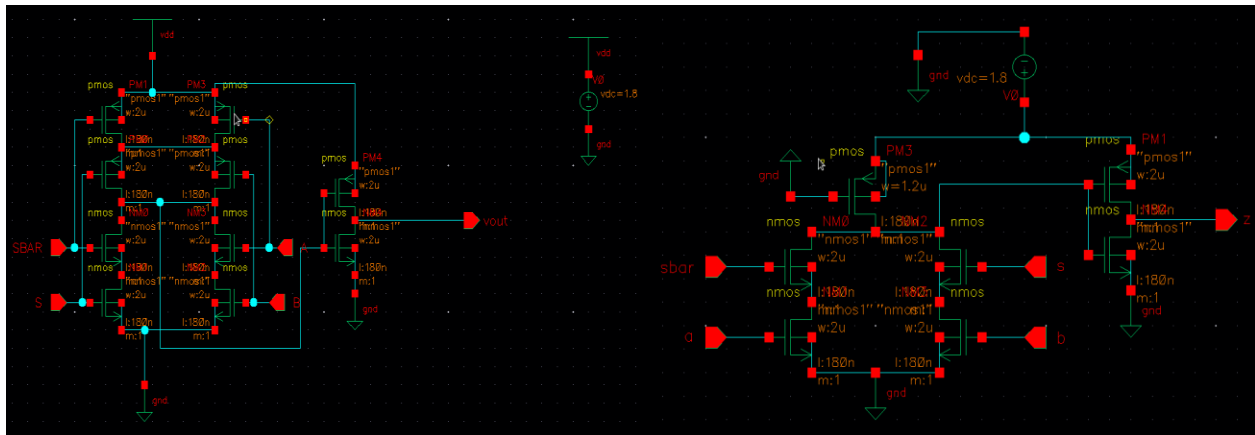
Barrel shifter is designed using Multiplexers. Barrel shifter design is for natural size like (2,4,8,16). This project is done on 8 bit barrel shifter which can Shift input by 0,1,2,3,4,5,6,7, bit. Three select lines are used as it is 8 bit barrel shifter i.e. S0, S1, S2. Basically barrel shifter is used with logical left shift operation which is controlled by select inputs.

$$16\text{-bit} \text{ --- } 16 \log_2 (16) = 16 \times 4 = 64$$

$$8\text{-bit} \text{ --- } 8 \log_2 (8) = 8 \times 3 = 24$$

## III. STATIC CMOS LOGIC AND PSEUDO NMOS LOGIC

A static CMOS gate is a combination of two networks, called the pull-up network (PUN) and The Pull- down network (PDN).



**Fig.2. 2:1 Mux using Complementary Logic (A) and pseudo NMOS logic (B)**

The below figure 2 shows a generic ‘N’ input logic gate where all inputs are distributed to both the pull up and pull down networks. The function of pull up network is drive the V<sub>dd</sub> towards output and function of the pull down network is to supply V<sub>ss</sub> to output. In pseudo NMOS logic

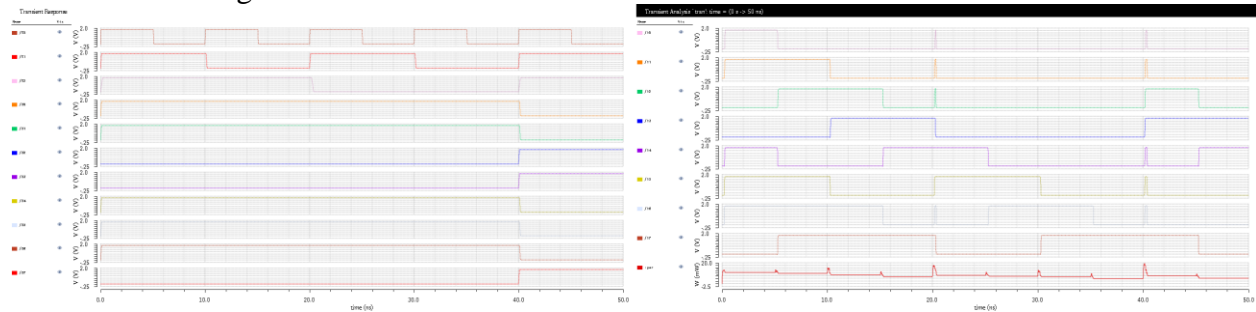
all the pull up network is replaced by single PMOS. Here the load device is single P transistor with gate connected to ground. So the area required is less than that of the static complementary network.

**IV. PROPOSED BARREL SHIFTER**

After analyzing all two technologies, it shows that complementary logic uses both pull up network as well as pull down network so that number of CMOS required is more. In pseudo NMOS logic all the PMOS are replaced by the single PMOS, hence the no. of MOS required is reduced. As the numbers of Transistors are reduced the power consumed by the CMOS is also reduced.

**V. SIMULATION AND PERFORMANCE ANALYSIS OF BARREL SHIFTER**

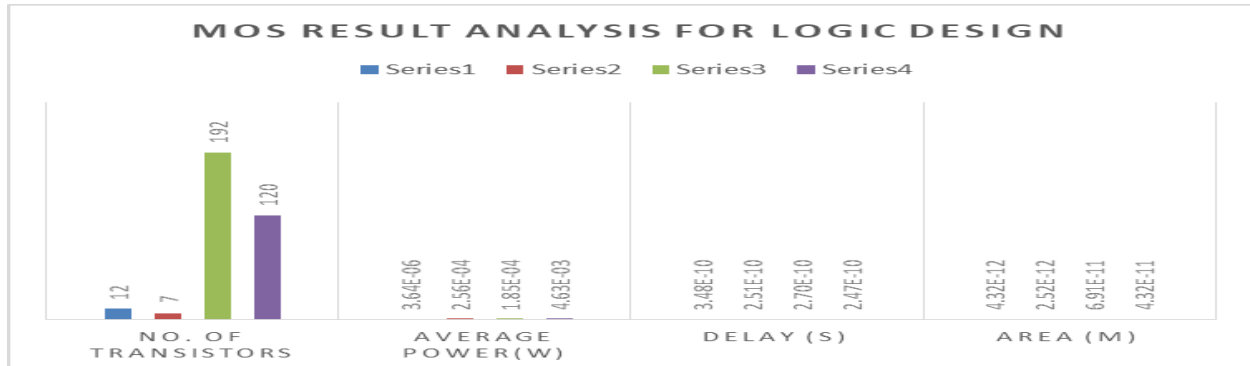
Barrel Shifter is designed and simulated using the CADENCE VIRTUOSO 6.1 tool at 180nm at Vdd level 1.8V. At first, 2:1 Mux is designed on both technologies i.e. both complementary logic and Pseudo NMOS logic at 180nm. Fig.3 shows the output waveform of 8 bit barrel shifter Pseudo NMOS logic.



**Fig.3: Output Waveform of 8bit Barrel Shifter using Pseudo NMOS Logic Area, Delay and Power Analysis**

As the numbers of MOS are reduced in Pseudo NMOS logic, ultimately Area is also optimized. Therefore the area of barrel shifter is also reduced which helps to reduced the area of chip of ALU. As the area is optimized the speed of the operation is increased. Number of MOS required to each circuit design is as shown in table.

**Table 1. MOS Result analysis for logic design**



## CONCLUSION

In this Paper, the barrel shifter is designed using complex logic structures and area of barrel shifter is reduced. By using CADENCE VIRTUOSO 6.1 tool power consumed by the each logic on 180nm is calculated and the reduced area, delay and power barrel shifter is proposed.

## RESULT

In VLSI, the major aspects of designing are Power, Speed and Area of the circuit. According to the design and simulation it is found that the area required for designing 8 bit barrel shifter using Pseudo NMOS logic reduces up to 62.5% than static CMOS Logic. In Power analysis, the average power dissipated in Static CMOS logic is less than Complementary logic by 1.31% on 180nm technology.

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