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RESEARCH ARTICLE

DESIGN OF LOW POWER / HIGH SPEED MULTIPLIER USING SPURIOUS POWER SUPPRESSION TECHNIQUE (SPST)

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Abstract — This project provides the experience of applying an advanced version of Spurious Power Suppression Technique (SPST) on multipliers for high speed and low power purposes. When a portion of data does not affect the final computing results, the data controlling circuits of SPST latch this portion to avoid useless data transition occurring inside the arithmetic units, so that the useless spurious signals of arithmetic units are filter out. Modified Booth Algorithm is used in this project for multiplication which reduces the number of partial product to n/2. To filter out the useless switching power, there are two approaches, i.e using registers and using AND gates, to assert the data signals of multipliers after data transition. The simulation result shows that the SPST implementation with AND gates owns an extremely high flexibility on adjusting the data asserting time which not only facilitates the robustness of SPST but also leads to a speed improvement and power reduction

Index Terms—SPST; Low Power Design; Modified Booth; FPGA; Verilog HDL

Full Text: http://www.ijcsmc.com/docs/papers/January2014/V3I1201406.pdf