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RESEARCH ARTICLE

Comparative Study of 6T and 8T SRAM Using Tanner Tool

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Abstract— In this paper we focus on the dynamic power dissipation during the Write operation in CMOS SRAM cell. The charging and discharging of bit lines consume more power during the Write "1" and Write "0" operation. 8T SRAM cell includes two more trail transistors in the pull down path for proper charging and discharging the bit lines. The results of 8T SRAM cell are taken on different frequencies at power supply of 1.5 V. The circuit is characterized by using the 130 nm technology which is having supply voltage of 1.5 V. Finally the results are compared with Conventional 6T SRAM cell. The power dissipated in low power 8T SRAM cell is reduced in comparison to conventional 6T SRAM cell. The result of the research has practical reference value for further study.

Keywords— SRAM, Tanner Tool, T-Spice, W-EDIT, IEEE

I. INTRODUCTION

SRAM is mainly used for the cache memory in Microprocessors, mainframe computers, engineering workstations and memory in hand held devices due to High speed and low power consumption. The need for low-power design is becoming a major issue in high-performance digital systems such as microprocessors [1], Digital Signal Processors (DSPs) and other applications. The increasing Market of mobile devices and battery powered portable electronic systems is creating demands for chips that consume the smallest possible amount of power. SRAM consist of almost 60% of Very Large Scale Integrated (VLSI) circuits. It is also said that memories are the biggest culprit for the power dissipation in any digital system and No digital system gets complete without memories.

Several techniques have been proposed to reduce the power consumption during Write operation of SRAM like, Segmented Virtual Ground Architecture for Low-Power Embedded SRAM [2], Low power SRAM design using half-swing pulse mode techniques [3] and A single-bit line cross-point cell activation (SCPA) architecture for ultra-low power SRAM's[4].Some other techniques which are used for low power SRAM

like Half-Swing Pulse-Mode Techniques[5] these techniques are used for reduce the power dissipation of the SRAM circuit. All these discussed papers are used extra circuitry for reducing the power consumption.

In this paper optimized SRAM cell contains two extra tail transistors in the pull-down path of the respective inverter to avoid charging of the bit-lines. These two trail transistor are controlled by an extra signal write select (WS). During read or write mode at least one of the tail transistor must be turned OFF to disconnect the driving path of respective inverters.

II. RELATED WORK

Karimi and Alimoradi [6]: Rapid growth in semiconductor technology has led to shrinking of feature sizes of transistors using deep submicron (DSM) process. As MOS transistors enter deep submicron sizes, undesirable consequences regarding power consumption arise. This can be done by using one PMOS transistor and one NMOS transistor in series with the transistors of each logic block to create a virtual ground and a virtual power supply. Notice that in practice only one transistor is necessary, because of their lower on-resistance, NMOS transistors are usually used.

Cheng and Huang [7]: they present a low-power SRAM design with quiet-bit line architecture by incorporating two major techniques. Firstly, the authors use a one-side driving scheme for the write operation to prevent the excessive full-swing charging on the bit lines. Secondly, they use a precharge free pulling scheme for the read operation so as to keep all bit lines at low voltages at all times. SPICE simulation on a 2K-bit SRAM macro shows that such architecture can lead to a significant 84.4% power reduction over a self-designed baseline low-power SRAM macro.

Ming et. Al. [8]: They describes a low-power write scheme by adopting charge sharing technique. By reducing the bitlines voltage swing, the bitlines dynamic power is reduced. The memory cell's static noise margin (SNM) is discussed to prove it is a feasible scheme. Simulation results show compare to conventional SRAM, in write cycle this SRAM saves more than 20% dynamic power.

III. STATIC RAM

SRAM or Static random Access memory is a form of semiconductor memory widely used in electronics, microprocessor and general computing applications. This form of semiconductor memory gains its name from the fact that data is held in there in a static fashion, and does not need to be dynamically updated as in the case of DRAM memory. While the data in the SRAM memory does not need to be refreshed dynamically, it is still volatile, meaning that when the power is removed from the memory device, the data is not held, and will disappear. There are two key features to SRAM - Static random Access Memory, and these set it out against other types of memory that are available: **The data is held statically:** This means that the data is held in the semiconductor memory without the need to be refreshed as long as the power is applied to the memory. **SRAM is a form of random access memory:** A random access memory is one in which the locations in the semiconductor memory can be written to or read from in any order, regardless of the last memory location that was accessed. Fig 1 shows the read/write operations of an SRAM. To select a cell, the two access transistors must be “on” so the elementary cell (the flip-flop) can be connected to the internal SRAM circuitry.

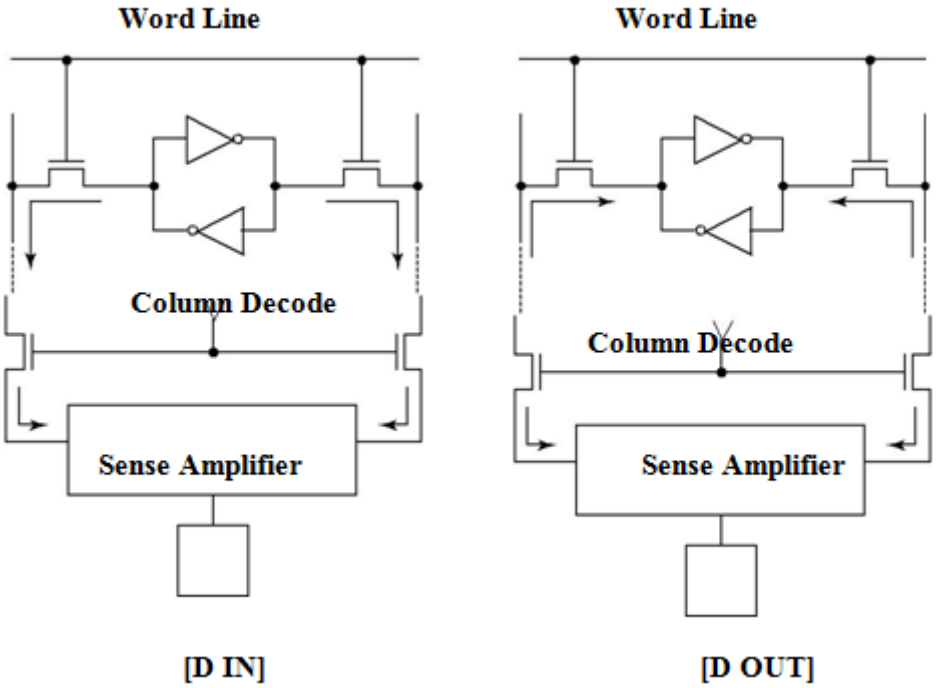

Fig. 1 Read/Write Operations

OPTIMIZED 8T SRAM CELL Schematic of 8T SRAM cell is shown in fig 2 In that we are using two more transistors M7 and M8 for reducing the power dissipation. WS signal is used for controlling the M7 and M8 during Write "0" and write "1" operation.

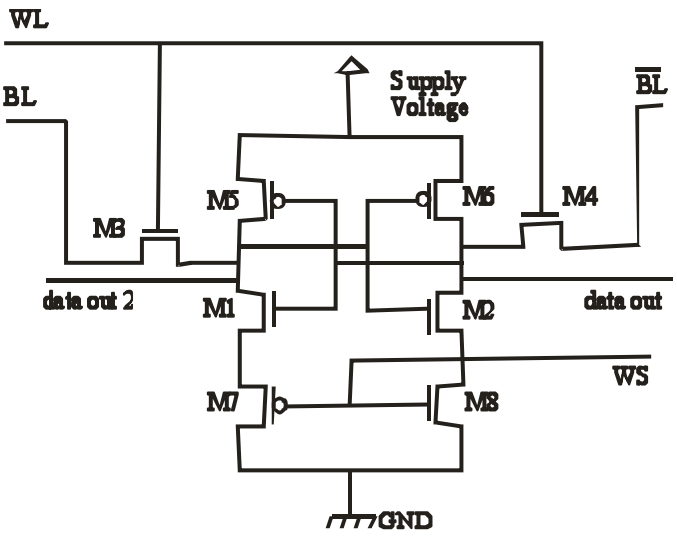

Fig. 2 Optimized 8T SRAM Cell

IV. **COMPARISON ON DIFFERENT FREQUENCY**

This section provides the detail simulation analysis of Low power SRAM cell for different frequencies. The dynamic power may be expressed as: $P=\alpha CV^2 f$.

A. SCHEMATIC DIAGRAM OF SRAMS (S-EDIT):

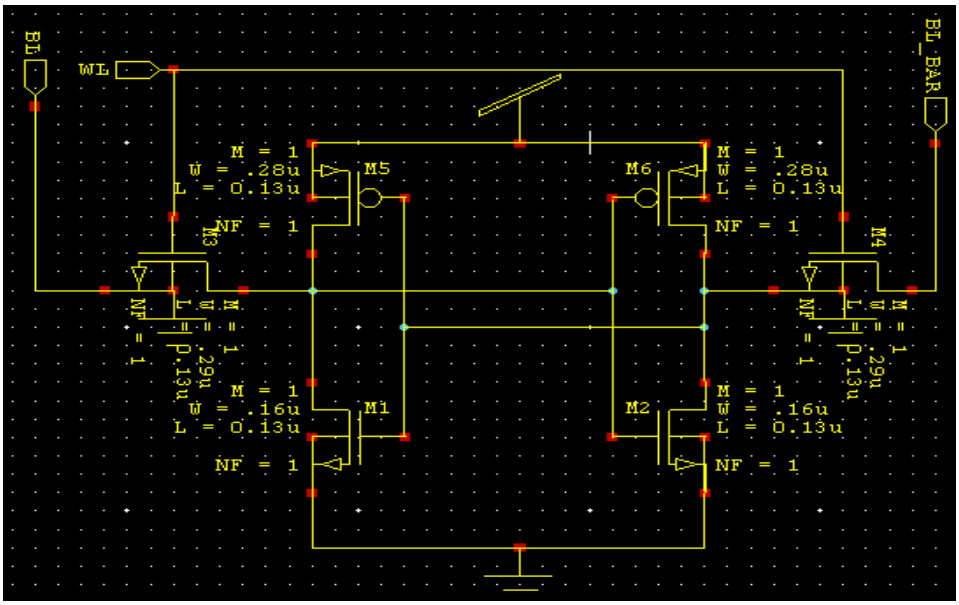

Fig. 3 Conventional 6T SRAM Cell (S-EDIT)

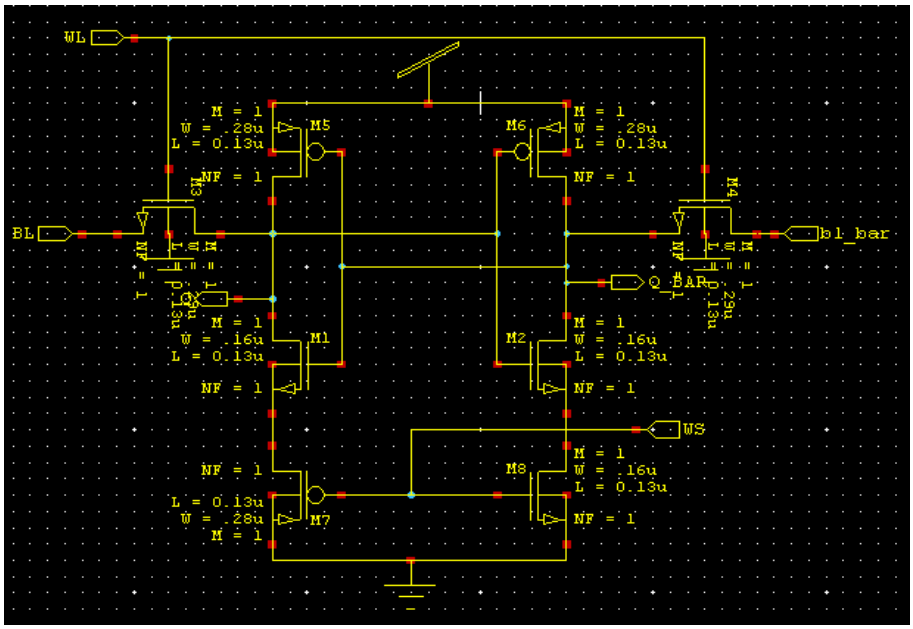

Fig. 4 Optimized 8T SRAM Cell (S-EDIT)

B. SIMULATION WAVEFORM OF SRAMS ON DIFFERENT FREQUENCIES (S-EDIT):

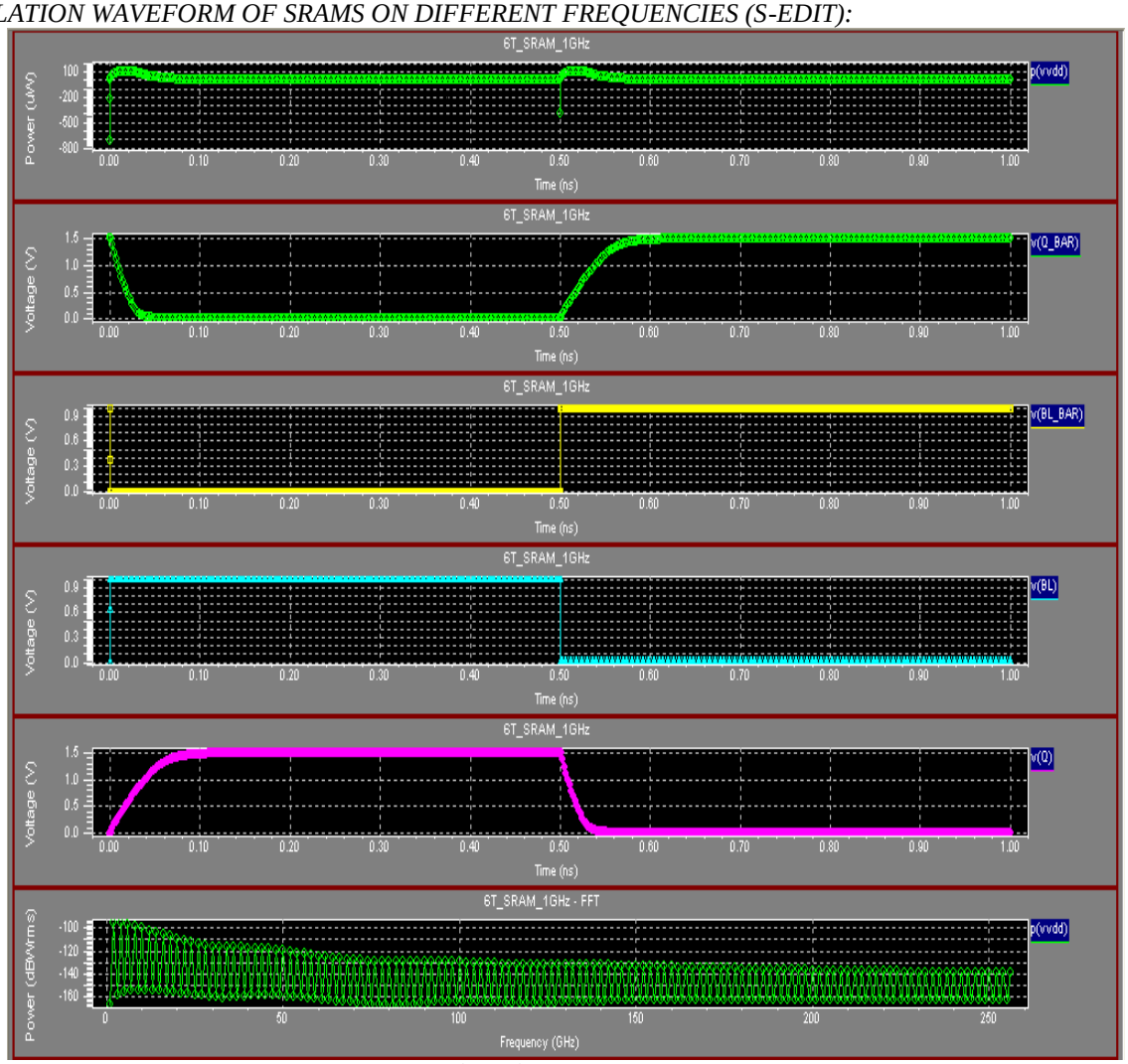

Fig. 5 Simulation Waveform of 6T SRAM at 1GHz (S-EDIT)

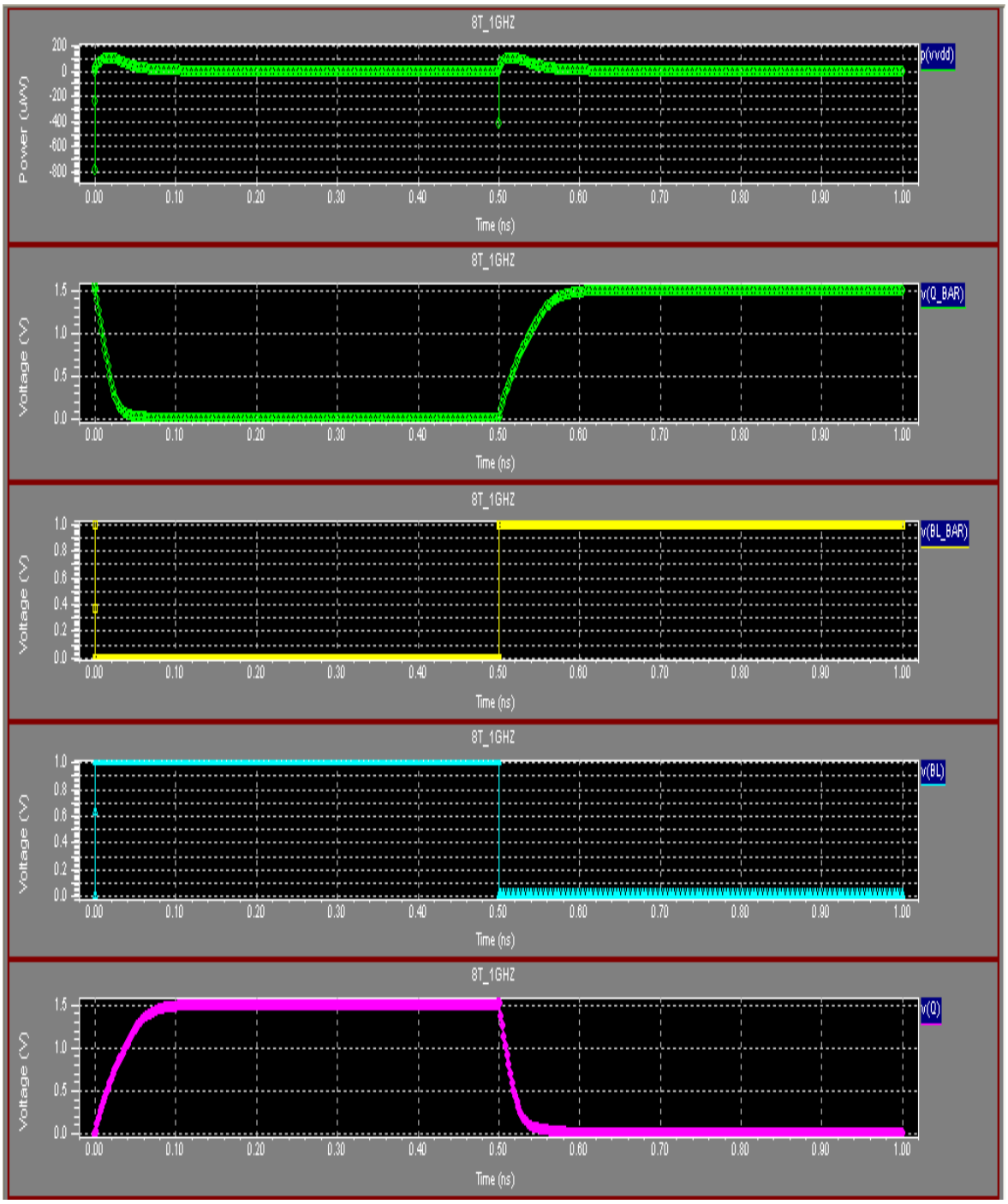

Fig. 6 Simulation Waveform of 8T SRAM at 1GHz (S-EDIT)

From the fig 4.7 it has been clear that for 1 GHz the charging time is less then discharging time. So due to increment in charging and discharging time with frequency the power dissipation will also increase.

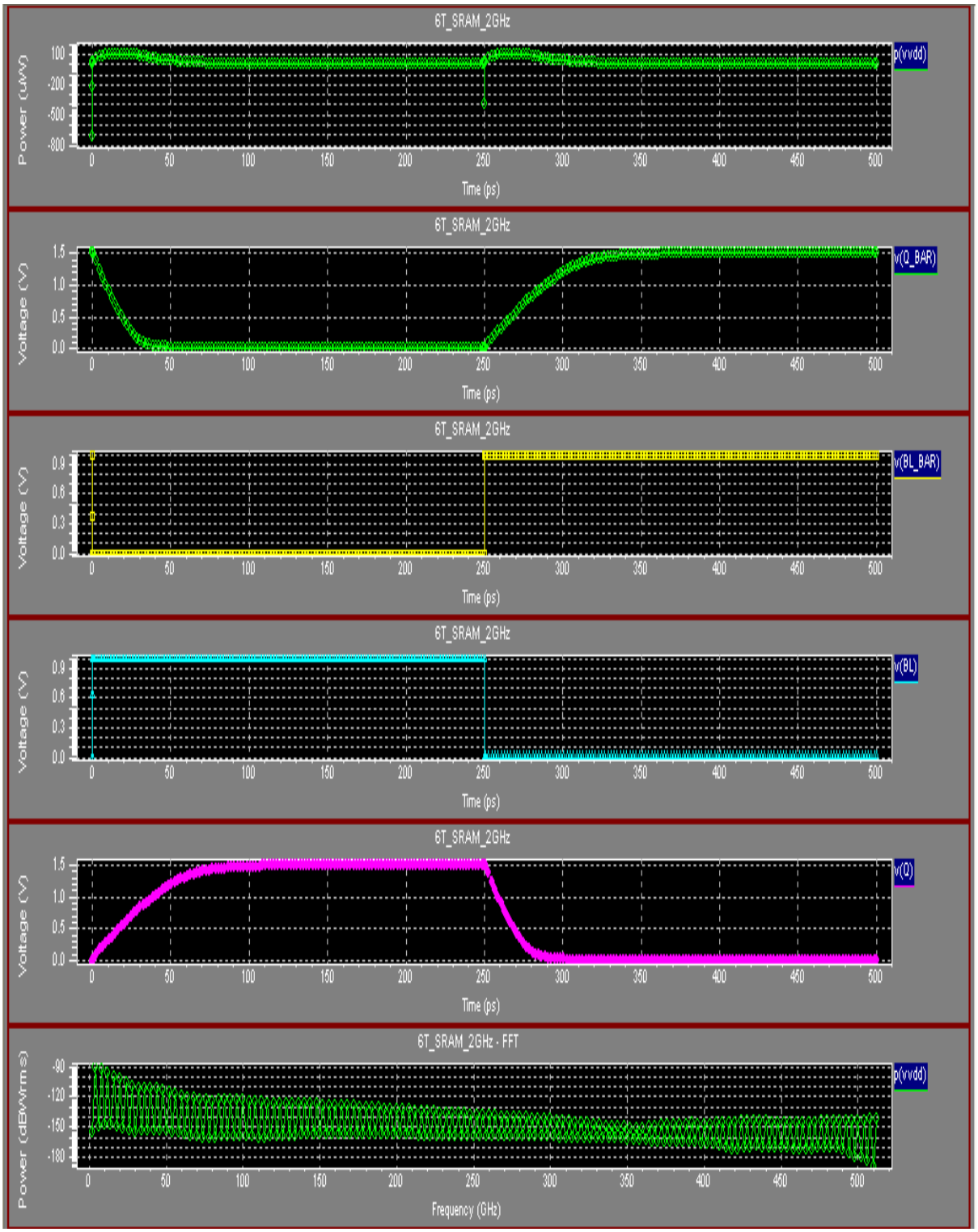

Fig. 7 Simulation Waveform of 6T SRAM at 2GHz (S-EDIT)

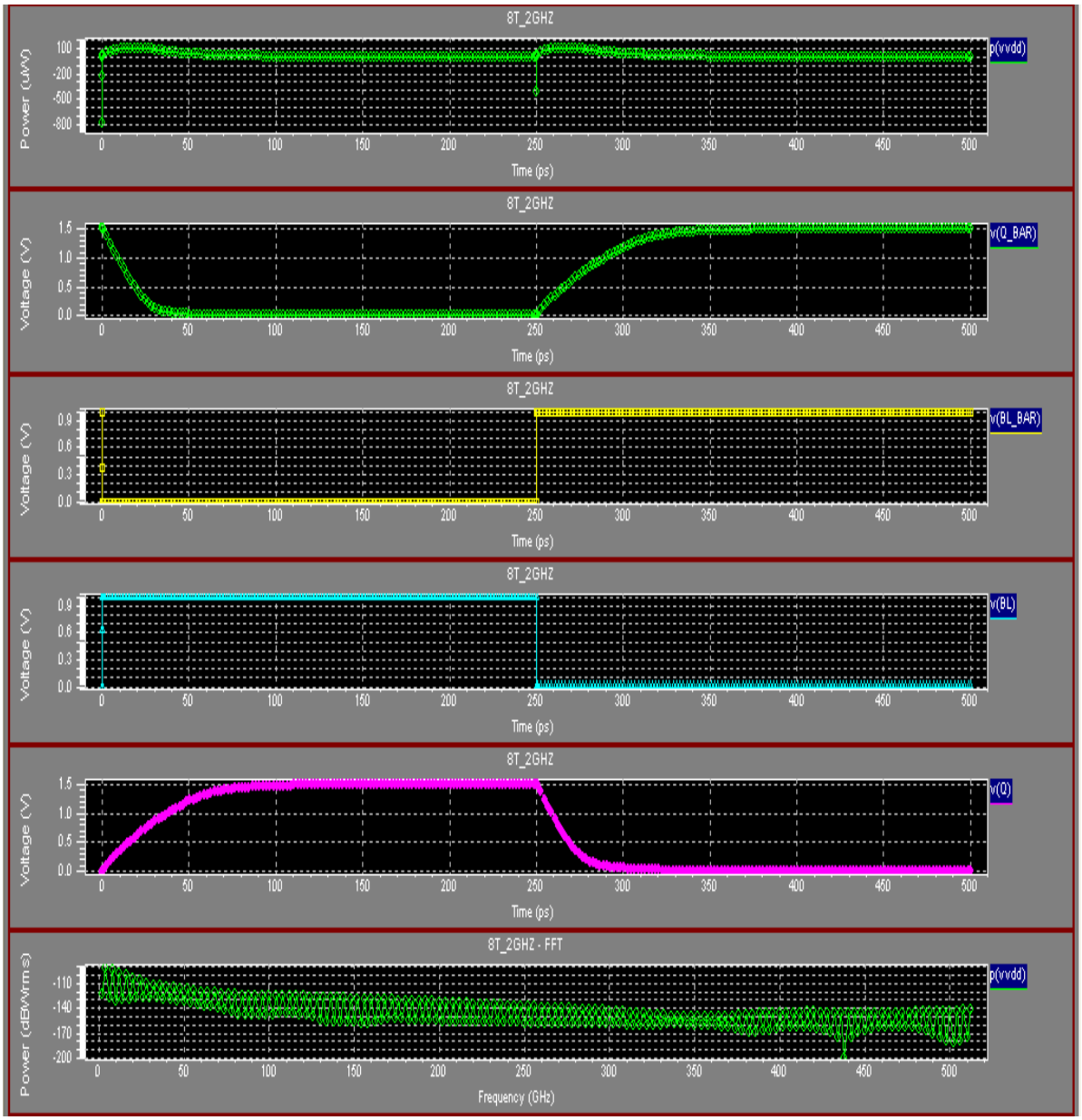

Fig. 8 Simulation Waveform of 8T SRAM at 2GHz (S-EDIT)

TABLE I
COMPARISION ON BAISES OF FREQUENCY

Frequencies	**Power Dissipation in 6T SRAM cell (µw)**	**Power Dissipation in 8T SRAM cell (µw)**
1 GHz	6.75	4.72
2 GHz	9.854	8.782

Write operation on different frequencies, are given in Table I. Our 8T SRAM cell dissipates lower dynamic power during the switching activity. In 8T SRAM cell the crosstalk voltage values are increased for bit lines, word line (WL) and for outputs in comparison to conventional SRAM cell but these Values can be controlled with the help of proper sizing of Width (W) and Length (L) of the transistor.

C. SIMULATION WAVEFORM OF AVERAGE POWER DISSIPATION AND DELAY (S-EDIT):

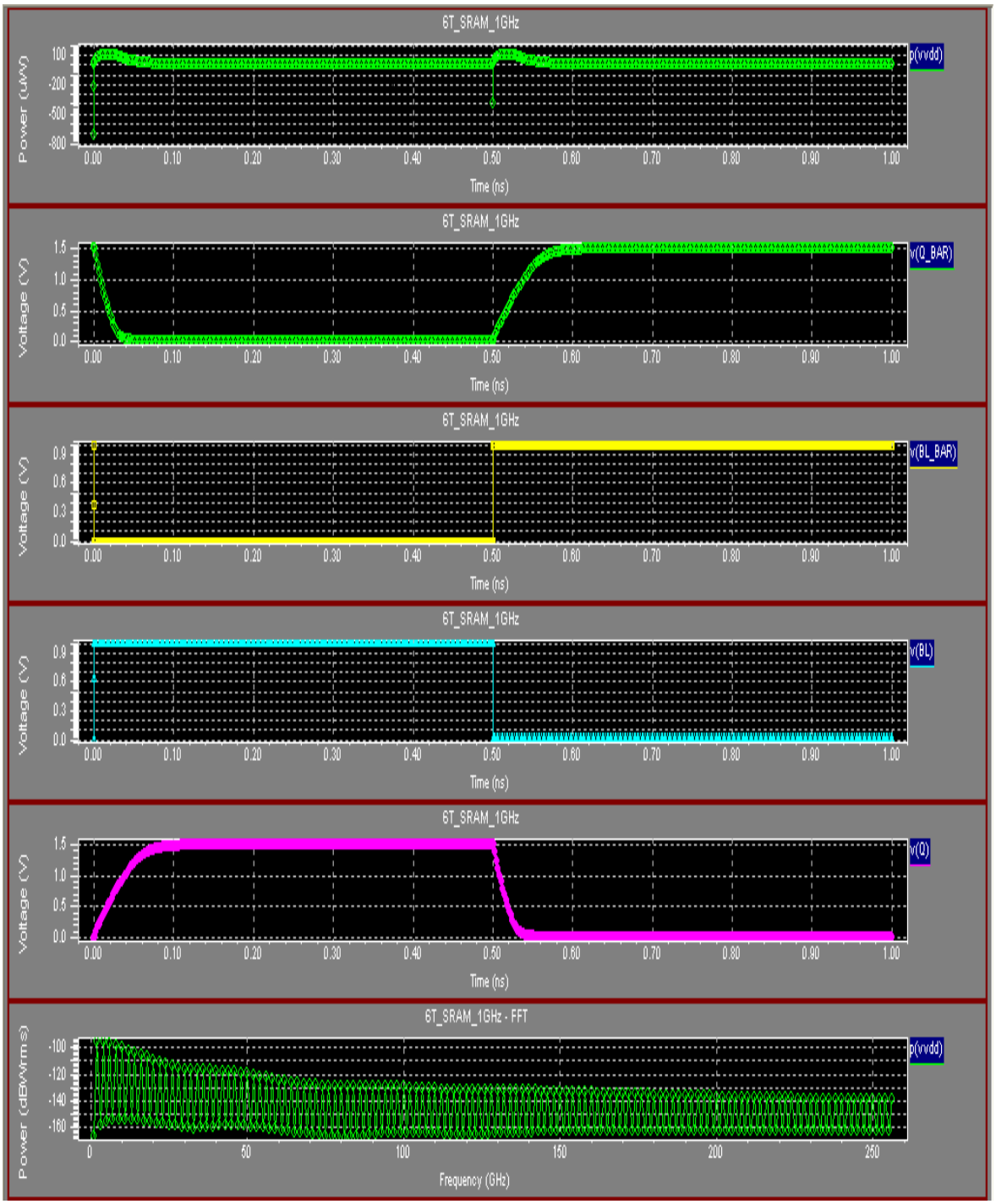

Fig. 9 Simulation Waveform of 6T SRAM (S-EDIT)

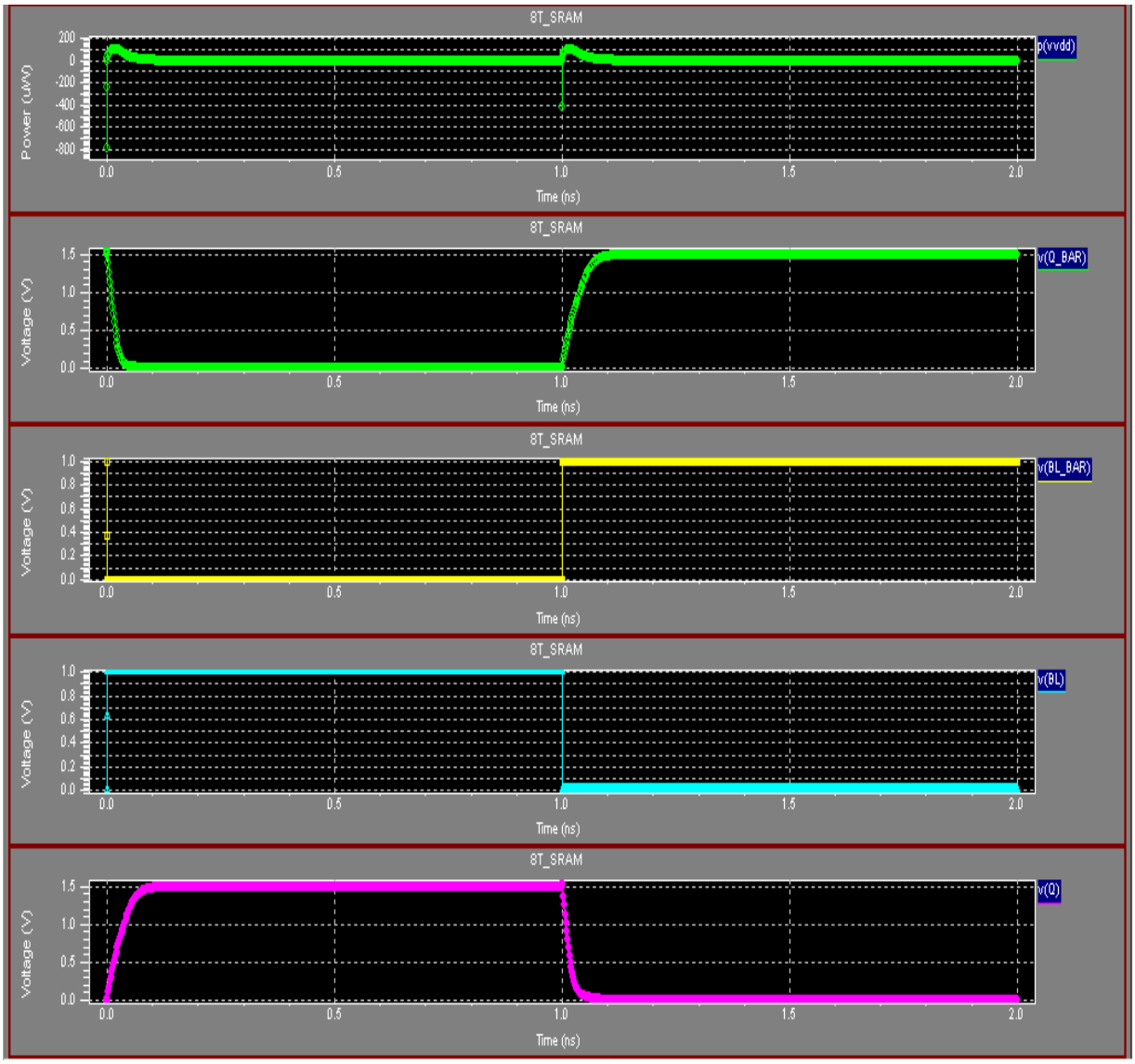

Fig. 10 Simulation Waveform of 8T SRAM (S-EDIT)

TABLE II
COMPARISION TABLE

Different SRAM cells	Average Power Dissipation	Delay
6T SRAM	6.75 µw	5.44 ns
8T SRAM	5.52 µw	3.86 ns

In our 8T SRAM cell as shown above we are preventing any single bit line from being discharged during write "0" as well as write "1" mode by proper selection of signal WS, which turn either M7 or M8 OFF. The comparison of conventional 6T SRAM cell and 8T SRAM cell is shown in table II

V. CONCLUSION

Most of the developed low-power SRAM techniques are used to reduce only read power. Since, in the SRAM cell, the write power is generally larger than read power. We have proposed an SRAM cell to reduce the power in write operation by introducing two tail Transistors in the Pull-down path for reducing leakages. Due to this Stack Transistors the power dissipation has reduced from 18 % in comparison to Conventional 6T SRAM cell. The 8T SRAM provides power efficient solution. There is also improvement in the delay in case of 8T SRAM cell is 29% faster as compared to the conventional SRAM cell. So the newly designed low power SRAM cell consume lesser power and can be said that it is a power aware cell which is acceptable in today's VLSI design market.

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