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Design and Implementation of High Performance 4-bit Dadda Multiplier using Compressor

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Abstract- Fast multiplication is an essential necessity of any high processing framework. Multiplier assumes a critical part in fast ASIC's and chip. Since Tree multiplier will prompts many-sided quality in its plan. The diminishment in incomplete item is done as late as conceivable in Dadda multiplier. For the most part Multipliers with less basic intricacy will enhance the speed and diminish the aggregate power dispersal. A regular Dadda multiplier utilizes 3:2 compressors or full adders and half adders in their fractional item decrease organize. In this work, faster column compression has been accomplished by utilizing higher request compressors. The proposed Dadda multiplier utilizes 4:2 compressors in their partial product reduction stages. The plan is actualized and implemented by CADENCE 180nm device.

Keywords: column compression, compressor, Dadda, PDP, Wallace,

I. INTRODUCTION

Multipliers are critical in the present advanced flag handling and for different applications. Numerous scientists have attempted and many are endeavoring to plan the multipliers which will enhance the outline parameters like – speed, low power utilization less range or mix of these in one multiplier by making them appropriate for various fast, low power VLSI usage. The basic idea of DADDA multiplier depends on the underneath framework shape appeared in Fig 1 The partial product is framed in the principal organize by AND stages which is delineated in Fig 2.

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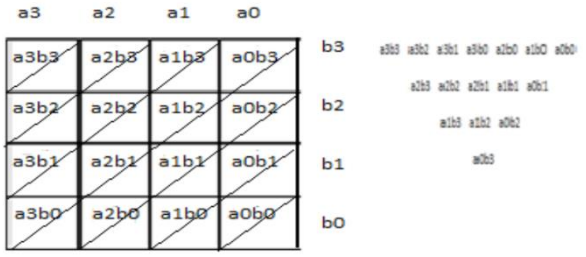

Fig No 1. Algorithm of Dadda multiplier

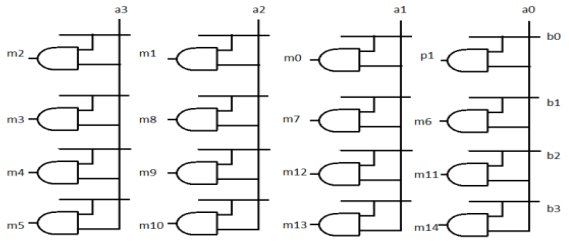

Fig 2. Partial product generation

The general procedure can be separated into three stages. The initial step is to create the partial product matrix. A case of 4*4 partial product matrix is given in Figure 3. Every halfway item is produced with an AND gate. Thus, 16 AND gates are required in a 4 by 4 multiplier. As a rule for N by N multiplier we require N*N AND gates. The second step is otherwise called the "decrease" step is to lessen the N lines of partial product bits to 2 bits that have a proportionate esteem. This progression has the most of the delay in a multiplier and here we concentrated on enhancing this deferral. The third step is to utilize a carry skip adder (CSA) to include the 2 rows and acquire their aggregate which is the result of the two information operands.

The goal is to outline and execute the Dadda multiplier utilizing compressors to lessen the power dissipation and to expand the speed.

II. METHODOLOGY

CMOS logic implementation

Dissimilar to Wallace multipliers that lessen however much as could reasonably be expected on each layer, Dadda multipliers endeavor to limit the quantity of gates utilized, and in addition input/yield delay. Due to this reason, Dadda multipliers are having more affordable lessening of partial product stage, yet it will accomplish a more ideal final product. So the structure of the reduction procedure of Dadda multiplier is represented by marginally more complex rules than in Wallace multipliers.

The means utilized as a part of regular Dadda augmentations are as per the following. multiply (sensible AND operation) each piece of w1, by each piece of w2 yielding outcomes, grouped by weight in segments. At that point decrease the quantity of partial product items by phases of full and half adders until the point when we are left with at most two bits of each weight. At last include the last outcome with a traditional adder. The decreases steps which is utilized as a part of regular Dadda multiplier can be comprehended by the dot diagram. The plan of 4 by 4 Dadda multiplier is given beneath.

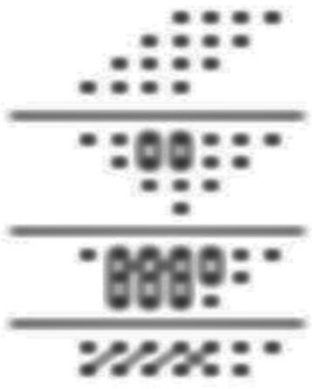

Fig no 3. Dot diagram

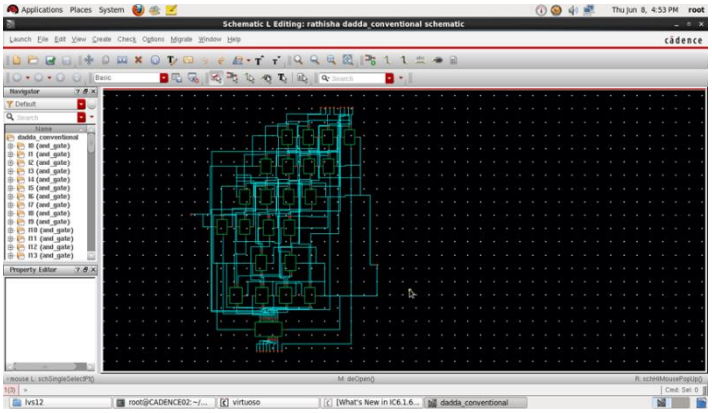

Fig no 4. Schematic of 4 by 4 Dadda multiplier

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III. IMPLEMENTATION

The following equations give the outcomes of the 4-2 compressor. The truth table is given figure 4.

TABLE 1
Truth Table of 4-2 Compressor

C_{in}	X_4	X_3	X_2	X_1	C_{out}	carry	sum
0	0	0	0	0	0	0	0
0	0	0	0	1	0	0	1
0	0	0	1	0	0	0	1
0	0	0	1	1	0	1	0
0	0	1	0	0	0	0	1
0	0	1	0	1	0	1	0
0	0	1	1	0	0	1	0
0	0	1	1	1	0	1	1
0	1	0	0	0	0	0	1
0	1	0	0	1	0	1	0
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0	1	1	1	1	1	0	0
1	0	0	0	0	0	0	1
1	0	0	0	1	0	1	0
1	0	0	1	0	0	1	0
1	0	0	1	1	0	1	1
1	0	1	0	0	0	1	0
1	0	1	0	1	0	1	1
1	0	1	1	0	0	1	1
1	0	1	1	1	1	0	0
1	1	0	0	0	0	0	1
1	1	0	0	1	0	1	0
1	1	0	1	0	0	1	0
1	1	0	1	1	0	1	1
1	1	1	0	0	0	1	0
1	1	1	0	1	0	1	1
1	1	1	1	0	0	1	1
1	1	1	1	1	1	0	0

$$Sum = x1 \oplus x2 \oplus x3 \oplus x4 \oplus Cin \qquad (2)$$

$$Cout = (x1 \oplus x2)x3 + \overline{(x1 \oplus x2)}x1 \qquad (3)$$

$$Carry = (x1 \oplus x2 \oplus x3 \oplus x4)Cin + \overline{(x1 \oplus x2 \oplus x3 \oplus x4)}x4. \qquad (4)$$

Fig no 4. Truth table and formulas of 4_2 compressor

We can do the execution of a 4-2 compressor is by utilizing two full-adder (FA) cells. Diverse plans have been proposed in the writing for 4-2 compressor. The block diagram of 4-2 compressor is given in Figure no 5 appears beneath. A 4-2 compressor can likewise be composed utilizing 3-2 compressors or full adder. It has two 3-2 compressors (full adders) in arrangement and inactivity of the basic way of 4 XOR delays as appeared in Figure no6. Another usage is given in a similar figure. This execution is better and has a basic way inertness of 3 XOR delay thus the basic way delay is diminished by 1XOR delay. The yield Cout is independent of the info Cin which quickens the summation of the partial products.

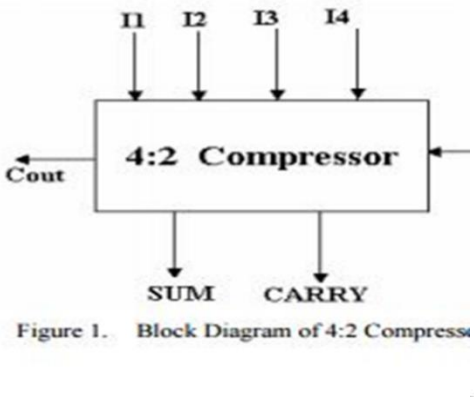

Figure 1. Block Diagram of 4:2 Compress

Fig no 5. Block diagram of 4_2 compressor

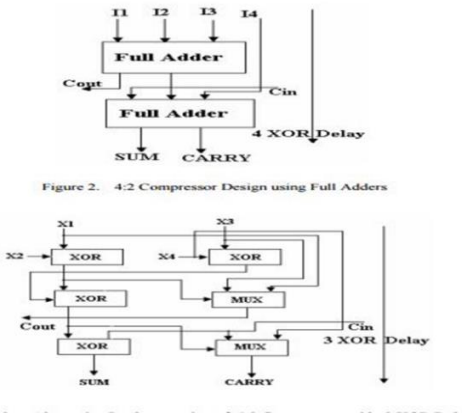

Figure 2. 4:2 Compressor Design using Full Adders

Fig no 6. 4_2 compressor design using full adders

A modified 4x4 Dadda multiplier utilizing compressors is composed. The components or the bits in the partial product matrix of Dadda multiplier are reworked to apply higher order compressors. Reworking on number of components is performed just in the sections that are beyond central column of the array of products. In light of the quantity of components in the segments of the partial product matrix the order the compressors have been picked. A 4x4 Dadda multiplier in light of higher order compressors will lessen the power utilization. Power utilization is diminished in light of the fact that the quantity of computational component (adders) utilized is decreased radically when higher order compressors are utilized. The outline of 4 to 2 compressor and 4 by 4 Dadda multiplier utilizing compressor is as demonstrated as follows.

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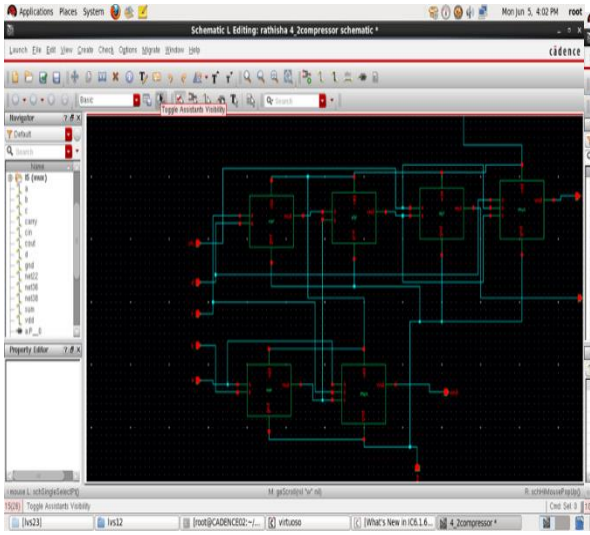


Fig no 7. Schematic of 4_2 compressor

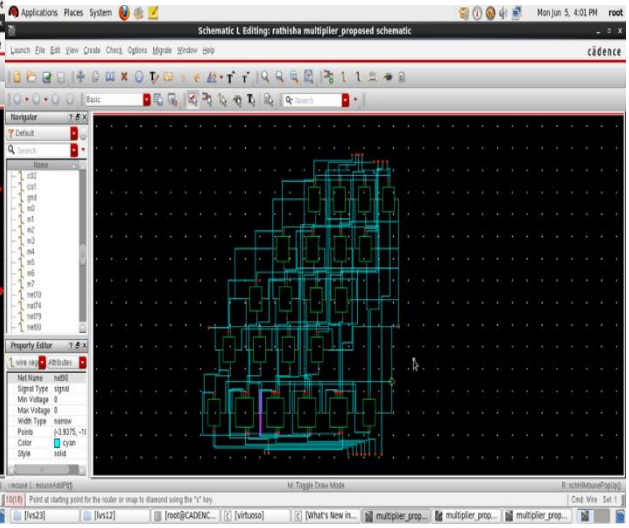
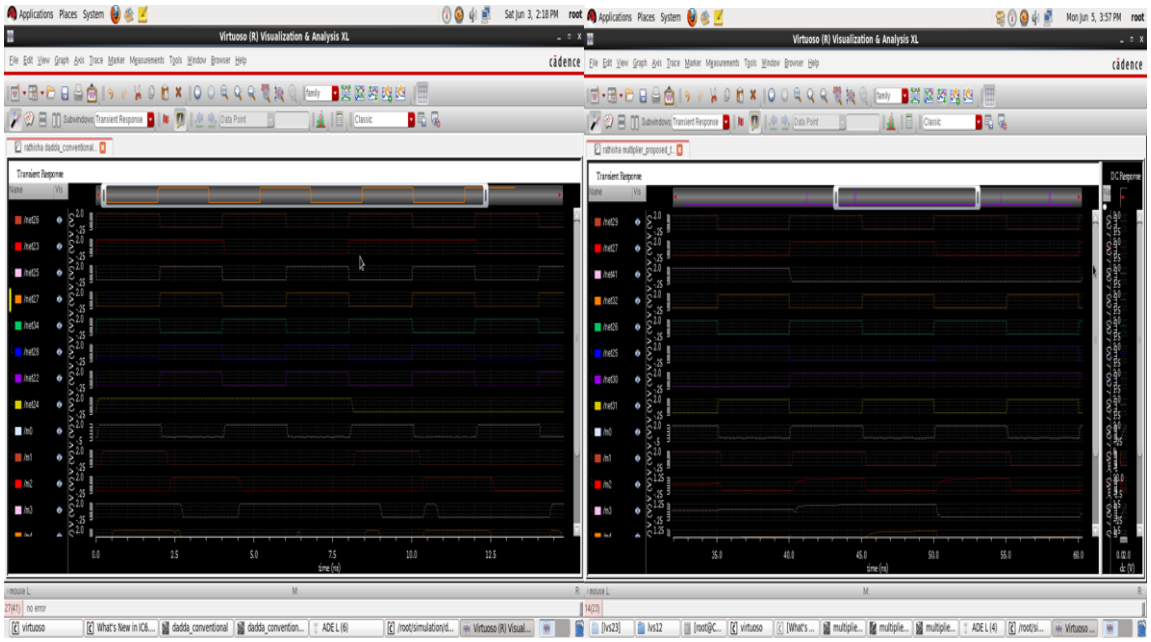


Fig no 8. Schematic of proposed multiplier

IV. EXPERIMENTAL RESULT

Output wave forms of conventional and proposed Dadda multipliers are given below.



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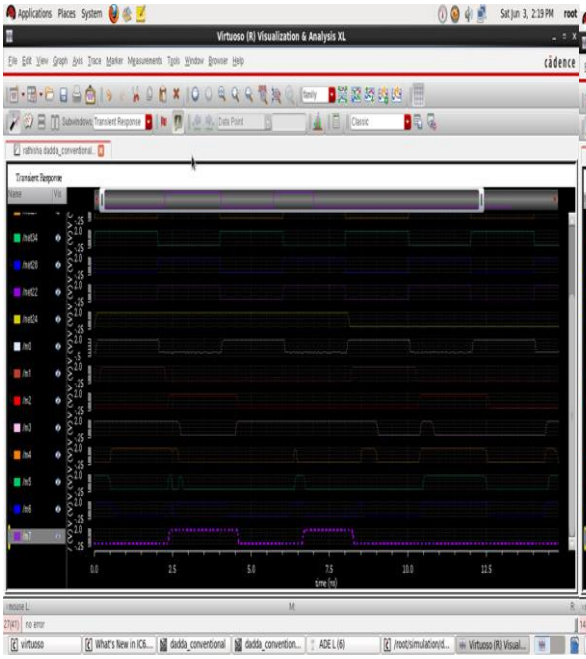

Fig no 9. Conventional multiplier output

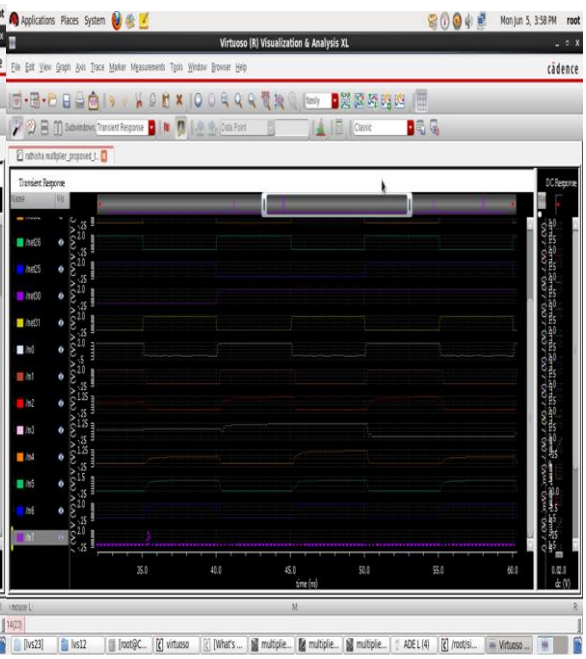

Fig no 10. Proposed multiplier output

Comparison of Performance Parameters for conventional and proposed multiplier

The traditional Dadda multiplier is having a power dissipation of 1.1mW. However, the multiplier which is outlined utilizing the proposed multiplier has a deferral of .66mW which implies a decrement of around .43. So the proposed multiplier lessens the power dissipation. Delay is an essential factor in the VLSI plan. The delay of customary Dadda multiplier is 359.3ps. Yet, the delay of proposed multiplier is 157.1. There is a decrease in 0.56. To plan traditional Dadda multiplier we utilized 376 transistor however in proposed multiplier there are just 244 transistor. So there is lessening in area in the proposed multiplier.The power delay product is a critical factor. The power delay product of proposed multiplier is less in the event that we contrast it and the regular multiplier power delay product. Every one of these parameters and its esteems are given in the beneath table.

PARAMETERS	**Conventional logic**	**Proposed logic**
1)Power(uW)	1172.9	662.2
2)delay(ps)	359.3	157.1
3) Chip area	More	Less
4)Number of transistors used	376 Transistors	244 Transistors
5) power delay product (pWsec)	0.421	0.104

Fig no 11. Comparison table

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V.CONCLUSION

The existing and proposed dadda multipliers are recreated utilizing cadence 180nm technology. The above table records the power and delay comes about for the regular and the proposed multipliers. It is observed that the change of 43.51% in control are accomplished for proposed structure when contrasted with existing 4x4 regular Dadda multipliers. A altered 4x4 Dadda tree multiplier in view of higher order compressors has been composed and implemented. The outcomes shows that proposed structure uses less power and area and transistor number. The PDP for proposed structure is minimum. Consequently the Dadda tree multiplier planned in using of higher order compressors is most appropriate for high performance multiplication.

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