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Design and Implementation of 4-bit Carry Skip Adder Using NMOS Pass Transistor Logic

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Abstract- In this paper the domain of VLSI design, the adders are always meant to be the most fundamental requirements for process of high performance and other multi core devices. It is founded that power dissipation is major problem in the electronics device so the goal of this project is to analyse and compare the performance of Carry skip adder using NMOS pass transistor logic configuration and the logic we used in this paper is NMOS pass transistor the configuration in terms of power dissipation, area, and delay. The paper also signifies more than 50% decrement in interconnect length, area, and number of transistor count while using a pass transistor logic in comparison of 4-bit carry skip adder with a CMOS logic configuration. Reduction in power dissipation up to 9.87% and delay also up to 60% and in transistor count is comes to reduce 35.2% is observed in pass transistor logic comparing to CMOS logic. It is implemented by using cadence RTL front end design tool. That is 180nm.

Keywords- CMOS logic configuration, NMOS pass transistor logic, power dissipation, area, delay.

I. INTRODUCTION

The Carry skip adder is a skip the logic in propagation of carry and its implementation is to speed up the additional operation and to adding the propagation of carry bit around portion of entire adder. In this paper the effect of change in architecture of carry skip adder in terms' of power dissipation, area, delay, is analyzed. The schematic diagram and additional truth table for carry skip adder have shown in Fig .1(a) and (b) respectively. The observed result indicates that the power dissipation, area, delay and other parameters vary with change in transistor technology. And this paper analysis the behaviour of carry skip adder in pass transistor logic and conventional CMOS logic architecture using cadence tool technology. And supply voltage 180nm and 1.8v are considered from experimental result. The result shows that carry skip adder is implemented in pass transistor

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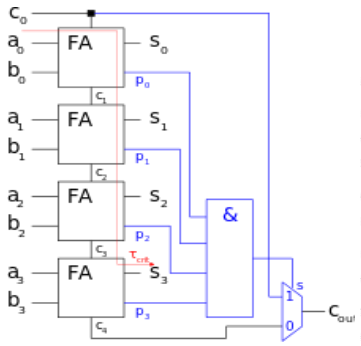
logic architecture perform better then comparison to CMOS logic configuration, reference(1), mainly in terms' of area, delay, power dissipation, and number of transistor counts.



Input Data A				Input Data B				Addition				
A4	A3	A2	A1	B4	B3	B2	B1	C	S4	S3	S2	S1
1	0	0	0	0	0	1	0	0	1	0	1	0
1	0	0	0	1	0	0	0	1	0	0	0	0
0	0	1	0	1	0	0	0	0	1	0	1	0
0	0	0	1	0	1	1	1	0	1	0	0	0
1	0	1	0	1	0	1	1	1	0	0	1	0
1	1	1	0	1	1	1	1	1	1	0	1	0
1	0	1	0	1	1	0	1	1	0	1	1	1

Fig.1 (a) Carry skip adder.

II. Methodology

CMOS logic; the digital circuit design is a most commonly used logic configuration but it has its own merits and demerits. Firstly the large numbers of transistors are required even in the implementation of small circuits. The bellow diagram shown that fig2 1bit full adder CMOS architecture its clear from the diagram that 28 transistors are required to implement the 1bit full adder and along with the AND logic gate also the OR logic gate to complete implementation of 4bit carry skip adder. Six transistors for AND gate total three AND gates, and for the OR gate six transistors are required. It can also understood from the circuit that large number of interconnects are used in this approach to connect the transistors. And in conventional process power dissipation delay and the transistor count are reduced and disadvantage is large number of interconnection are required and the cost is high where compare to pass transistor logic.

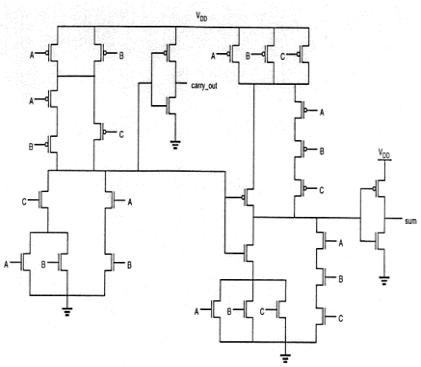


Fig2 1bit full adder

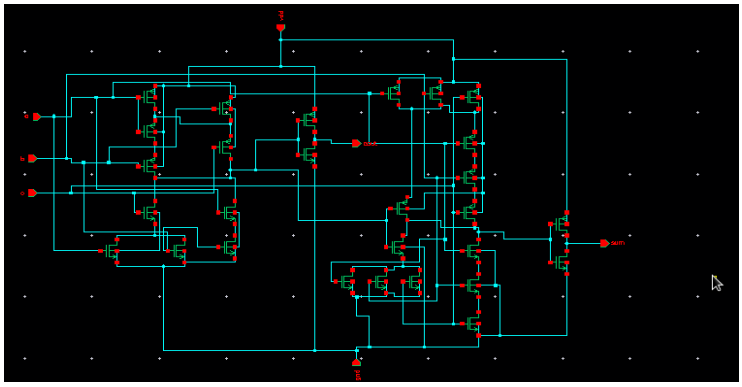


fig3 conventional full adder 28transistors

III. Implementation

Pass Transistor logic; Existing method to Implementation of carry skip adder in using pass transistor logic configuration and its requires the 18 NMOS transistors are required to complete the 1bit full adder and also for the AND gate only four transistors and for the OR gate only four transistors are requires. It means that number of transistors are used in pass transistor logic architecture is less then (50%) half of the transistors where used in CMOS logic configuration of carry skip adder. So the area is consumption is 50% less using pass transistor logic architecture.

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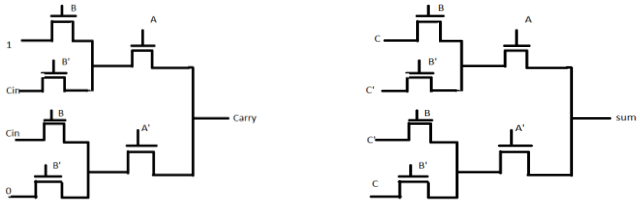
Sum & Carry, using pass transistor logic



In proposed block diagram there are four one bit full adders. And three AND gate logic blocks and also one OR gate logic block are used to implement and design the carry skip adder using pass transistor logic. And comes to a single bit (1bit) full adder design first we consider the truth table shown bellow and from the truth table hence we get the logical transistor level circuit diagram and its shown bellow one for SUM and another one for CARRY and this type of logic comes from the Pass transistor logic. The pass transistor logic working an control signal so we consider in truth table for input side A,B,C and for output side SUM,CARRY. We taken B, B' and A, A' as control signal and Cin is the taken as the input to determine the SUM there will be divided into those case are.

Case 1:- When A=0, and B=0. From the truth table of full adder that is clear that SUM will be follow input Cin, And the CARRY is 0 (zero).

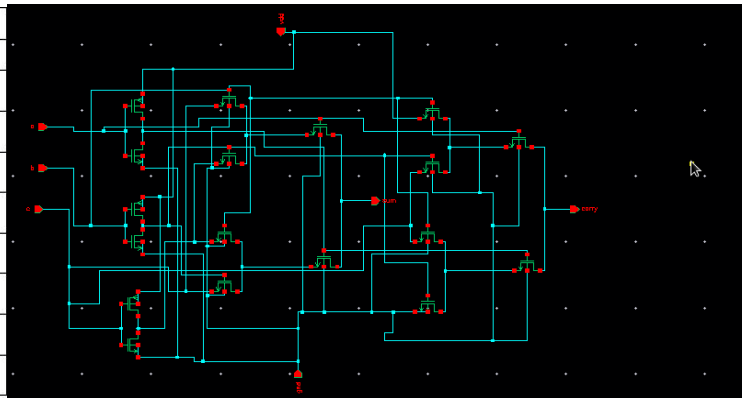
Case 2:- When A=0, and B=1. From the truth table of full adder that is clear that SUM will be complement of input Cin, and the CARRY follows the input signal Cin.

Case 3:- When A=1, and B=0. From the truth table of full adder that is clear that SUM will be complement of input Cin, and the CARRY follows the input signal Cin.

Case 4:- When A=1, and B=1. From the truth table of full adder that is clear that SUM will follow the input Cin, and the CARRY 1(one).

This SUM and CARRY are designed using Nmos pass transistor logic which is given in the bellow figure. For SUM we used 12 transistors and for the CARRY we used 10 transistors. Since we used Nmos logic we can design a diagram of full adder using pass transistor logic to reduce area, connectivity, delay and reduces the number of transistor in the design process. The bellow diagram shows that SUM and CARRY using pass transistor logic.

Input			Output	
A	B	Cin	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1



NMOS pass transistor logic 1bit full adder 18trnsisitor (fig 4)

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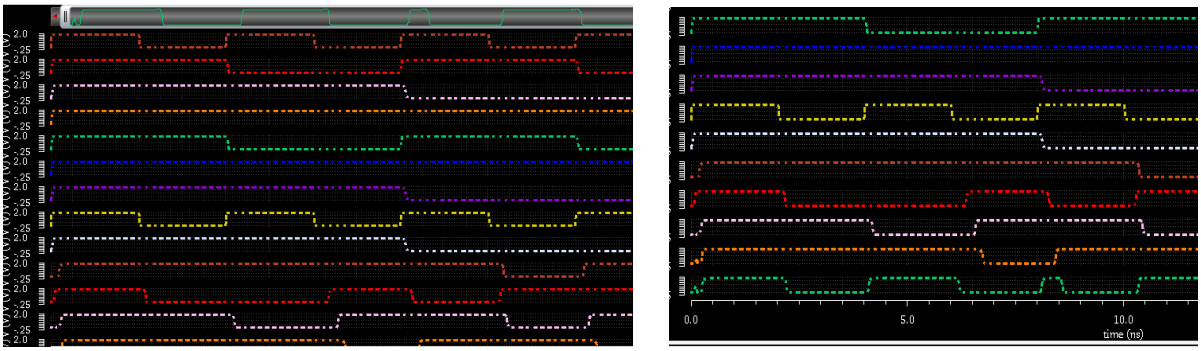
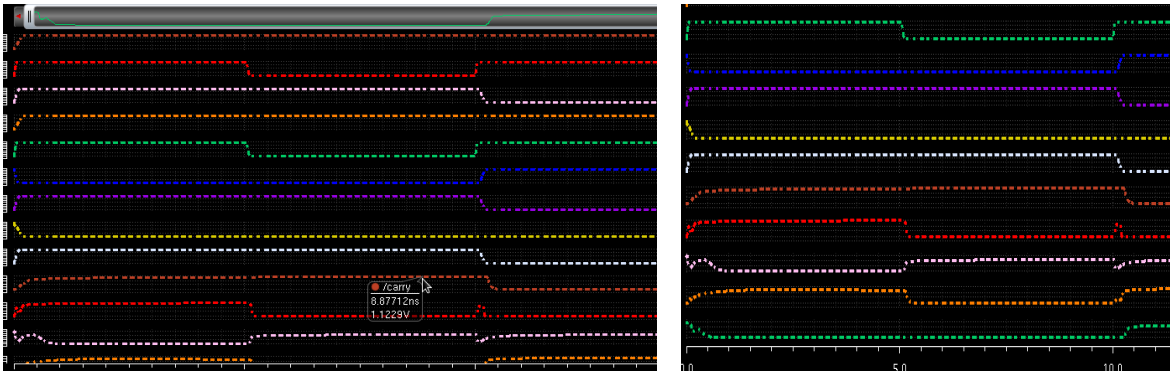
IV. Experimental Result

Comparison of CMOS logic architecture and NMOS Pass transistor logic, the bellow fingers shows the wave form result of both CMOS and pass transistor logic. Bellow shows wave forms are conventional result, here we can take one example look at the fig a, first signals are high (1) all input signals are (a1. A2, a3, a4) 1,1,1,1, and (b1, b2, b3, b4,) 1,1,1,1 carry is 1, and in the output side result (1, 1,1 1,) and the carry must be 1 high we can seen in the wave form of both a& b fig it's in CMOS logic configuration , while using NMOS pass transistor logic configuration wave forms of a&b, we can seen the input side a1, a2, a3, a4(1111), and b1, b2, b3,b4(1111), carry is one (1)high and the output is (1111). We can take one more example with different input number in input a1, a2, a3, a4(1011), and b1,b2,b3,b4 (0111) the output of this example is (0011) and the carry bit is high(1), it's for CMOS logic configuration, and for the using of NMOS pass transistor logic a1,a2,a3,a4(1011) and b1,b2,b3,b4(0111) carry is (1), for the output (0011), hence in the result we reduced area of the circuit and the power dissipation also with the delay, Using of this Nmos pass transistor logic.

Wave form result of both cmos logic and pass transistor logic



Output wave form of CMOS carry skips adder conventional (fig5)a and b



Proposed Carry skip adder output wave form using NMOS pass transistor logic. (fig6) a&b

Comparison Performance Parameters for CMOS and NMOS pass transistor logic configuration

Parameters'	Using CMOS logic	Using Nmos pass transistor logic
1)Power(uW)	320.9	289.2
2)delay(ps)	194.46	78.84
3) Chip area	More	Less
4)Number of transistors used	136 Transistors	88 Transistors

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5)overall performance	Overcomes CMOS Techniques	Equivalent to transmission gate
6) Power Delay Product(PDP)(pWsec)	0.062	0.022

V. CONCLUSION

In this proposed carry skip adder designed with NMOS pass transistor logic it consists of power, delay and area and its result to reduce the number of transistors and area35.2% ,and delay 60% in this implementation of carry skip adder and number of transistors are reduced and the connectivity will going to reduced with chip area, and 50% decrement in interconnect length compare to convention diagram of carry skip adder Full adder are used so that the complication of design is reduced and total designed power is saved.

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