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Software Implementation of Flying Capacitor Clamp Three Level Inverter Drive for Induction Motor

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Abstract— This paper is a simulation study of modulation strategies in three-phase three-level flying capacitor inverters in MATLAB Simulink. The flying capacitor multilevel converter is a recently developed converter topology assuring a flexible control and modular design. To improve the performance of Flying Capacitor Multilevel Inverter (FCMLI) implement the switching pattern selection scheme. This scheme reduces capacitor voltage fluctuation. This method is developed for sinusoidal voltage generation using the sinusoidal pulse width modulation technique the computer model allows a thorough investigation of all possible switching pattern permutations that produce the desired output and maintain steady state capacitor voltage balancing. Results show that the total harmonic distortion in a sinusoidal synthesised output can be minimised by the correct selection of the switching mode sequence.

Keywords— "Multilevel Inverter, Modulation Technique, Flying Capacitor multilevel converters (FCMLC), MATLAB Simulink model"

I. INTRODUCTION

Increasing demand for industrial power converters and some of interesting advantages of multilevel inverters such as low distortion in output voltage with relative low switching frequency, low harmonic and electromagnetic interference (EMI), attracted researcher attentions. Up to now, several topologies of multilevel inverter are presented. The main applicable topologies are Diode Clamped Inverter (DCI), Flying Capacitor Inverter (FCI) and Cascaded Multilevel Inverter (CMI). In order to achieve this higher power rating, the voltage and current capabilities of the devices used in the converter need to be increased. Current insulated gate bipolar transistor (IGBT) technology ex-tends up to 6.5 kV 900 A per switching device[2].

Meynard and Foch introduced a flying-capacitor-based inverter in 1992.The flying capacitor inverter have many attractive properties for medium voltage applications, including in particular the advantage of transformer less operation, and the ability to naturally maintain the cell capacitor voltages at their target operating levels[2]. One of the main reasons for

using the multilevel flying-capacitor inverter is to operate at voltages higher than the individual power switch blocking capability. Safe operation entails keeping the cell- capacitor voltage differences within restricted voltage bands and so the capacitor voltages are balanced. The flying-capacitor inverter can operate with inherent capacitor voltage balancing[3]. The most common and popular technique of digital pure-sine wave generation is sine pulse-width-modulation (SPWM). The SPWM technique involves generation of a digital waveform, for which the duty-cycle is modulated such that the average voltage of the waveform corresponds to a pure sine wave. The simplest way of producing the SPWM signal is through comparison of a low-power reference sine wave with a triangle wave.

II. PROPOSED METHODOLOGY

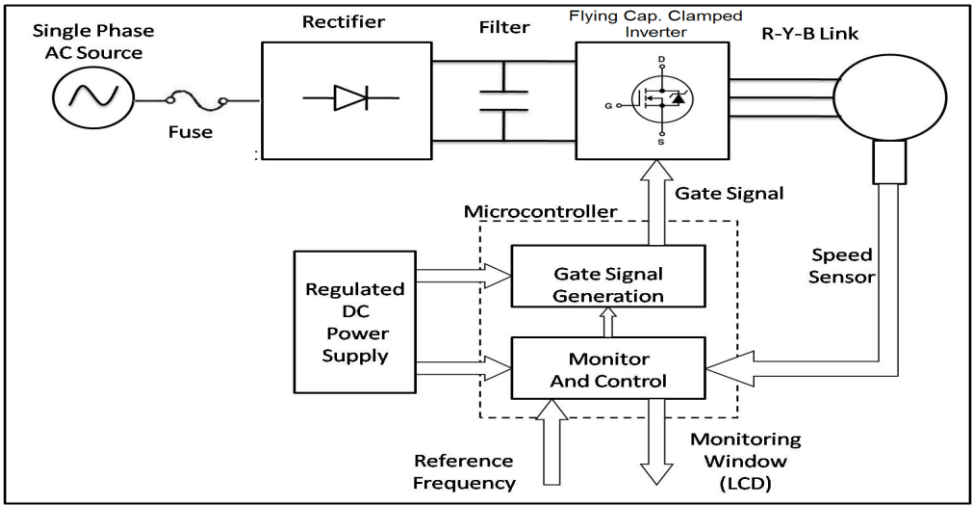

Fig.1 Block Diagram

An Adjustable Speed Drive(ASD) is supplied from three or single phase grid. It consists of a diode rectifier, DC link filter and an inverter. The rectifier converts supply AC voltage into DC voltage. The DC voltage is filtered by a capacitor in the DC link. The inverter converts the DC to an variable voltage, variable frequency AC for motor speed or (torque/current) control. The rectifier section of an ASD, called the front end, is responsible for generating current harmonics into the power supply system. Therefore, to reduce the total harmonic distortion (THD) of phase current it is necessary to add additional choke inductances. The FCMLI requires a large number of capacitors to clamp the device (switch) voltage to one capacitor voltage level. Provided all the capacitors are of equal value, an *n*-level inverter will require a total of $(n\text{-}1)\times(n\text{-}2)/2$ clamping capacitors per phase leg in addition to $(n\text{-}1)$ main dc bus capacitors. The size of the voltage increment between two consecutive legs of the clamping capacitors defines the size of voltage steps in the output waveform.

Let us consider the group of capacitors in a single clamping leg as one equivalent capacitor, then for an n level inverter, if the voltage of the main dc-link capacitor is *V*dc, the voltage of the innermost capacitor clamping the innermost two devices is $V\text{dc}/(n\text{-}1)$.The various switching strategies that have been proposed for synthesizing output voltage with minimum distortion, sinusoidal pulse width modulation (SPWM) strategy is employed here. In this method, a number of triangular waveforms are compared with a controlled sinusoidal modulating signal and the switching rules for the switches are decided by the intersection of the carrier waves with the modulating signal. For a 5-level inverter, a modulating signal and 4 carrier waves are required for each phase of the inverter. The modulating signal of each phase

is displaced from each other by 120°. All of the carriers have the same frequency *fc* and the same amplitude *Ac*, while the modulating signal has a frequency of *fm* and amplitude of *Am*. *Fc* should be in the multiples of three-times to that of *fm*. This is required such that all the modulating signal of all the three phases see the same carriers, as they are 120° apart.

III. SWITCHING TECHNIQUE

To synthesise a sinusoidal waveform the flexibility of the multiple voltage levels allows simple staircase control, whereby each voltage level is applied across the load at a predefined electrical angle in a fundamental cycle. The quality of the output voltage is an important criterion in selecting the control angles. These angles are defined, in general, to give a low level of total harmonic distortion (THD) whilst achieving the desired fundamental amplitude. In addition for three-phase applications, the magnitudes of low-order harmonics should be low. Furthermore the control must decide on which switching state to select at each voltage level since for a flying-capacitor inverter there are more than one switching modes available for the same intermediate voltage levels. The selection should obey the following three conditions. Allowing one independent switch changing state per voltage transition maintaining capacitor voltage balancing Maintaining equivalent switching device usage.

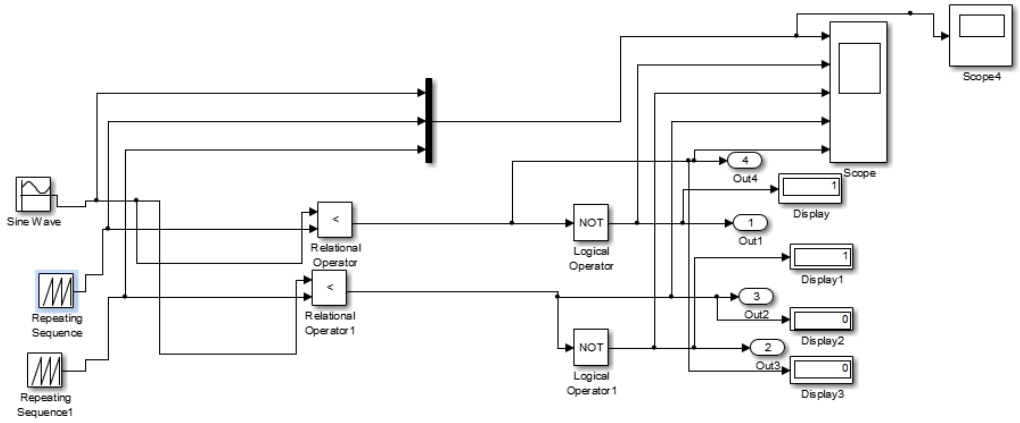

Fig. 2 Switching Sequence of 3 Level FCCMLI**.**

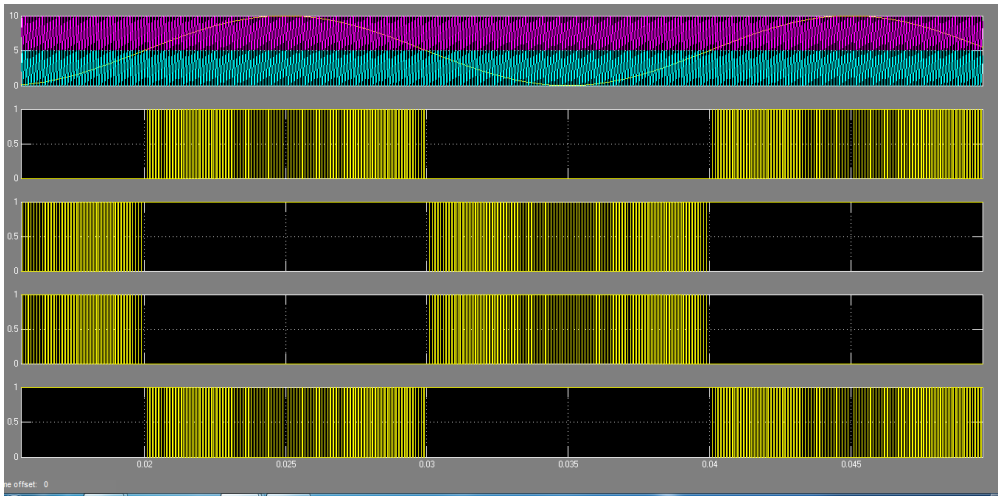

Fig. 3 Switching waveform of FCCMLI

IV. SIMULATION MODEL

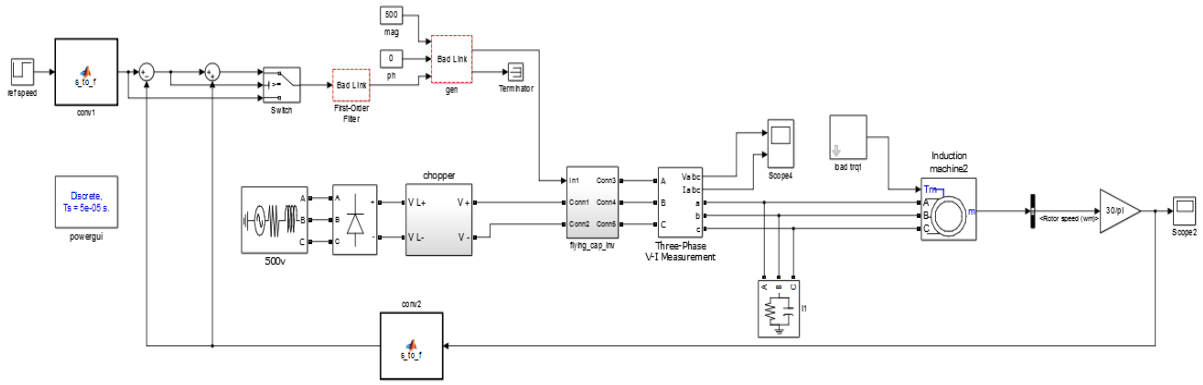

Fig.4 MATLAB Simulation model for three level inverter drive

Digital computer simulation model using MATLAB-SIMULINK has been developed to test the proposed FCCMLI fed IM drive. Simulation circuit diagram of the system is shown in figure .simulation model consist of The FCCMLI fed drive system consists of a three-phase diode bridge rectifier, sinusoidal wave generator, filter capacitor, Flying capacitor clamp three level inverter, three phase V-I measurement three-phase Induction Motor and feedback system. The speed increases linearly and reaches the rated speed 900rpm and 1200rpm at steady state in 0.85 s. At starting, the torque increases and reduces to a minimum value when the speed reaches the rated value. The THD value is limited to 30.29% is obtained the rotor reaches the desired speed without any oscillations. The output voltage of the inverter is balanced in less THD[8].

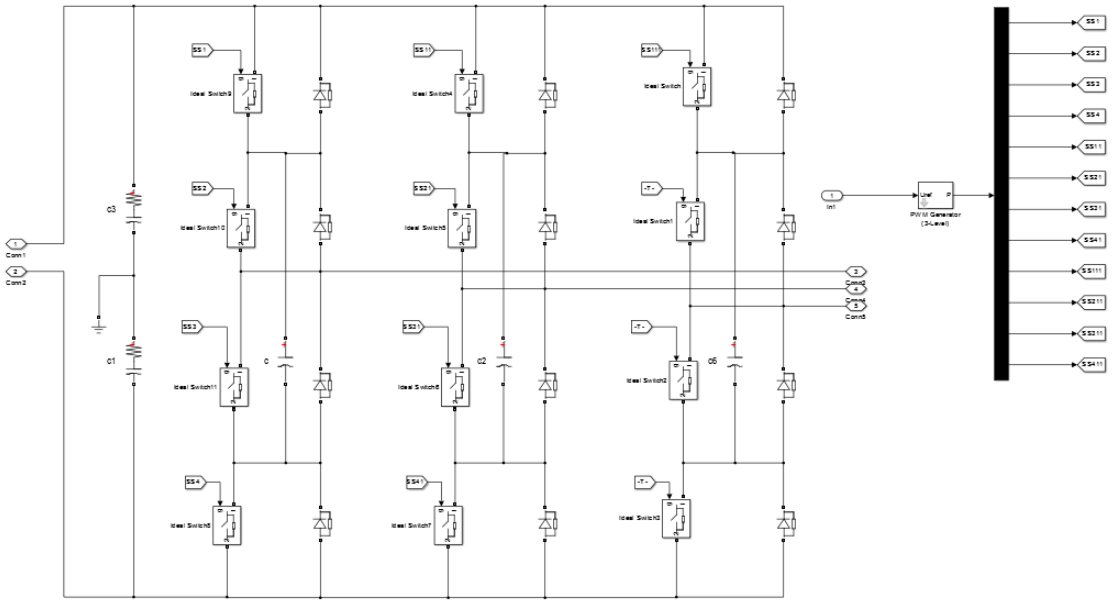

Fig. 5 MATLAB Simulink model 3 – level FCCMLI

V. SIMULATION RESULTS

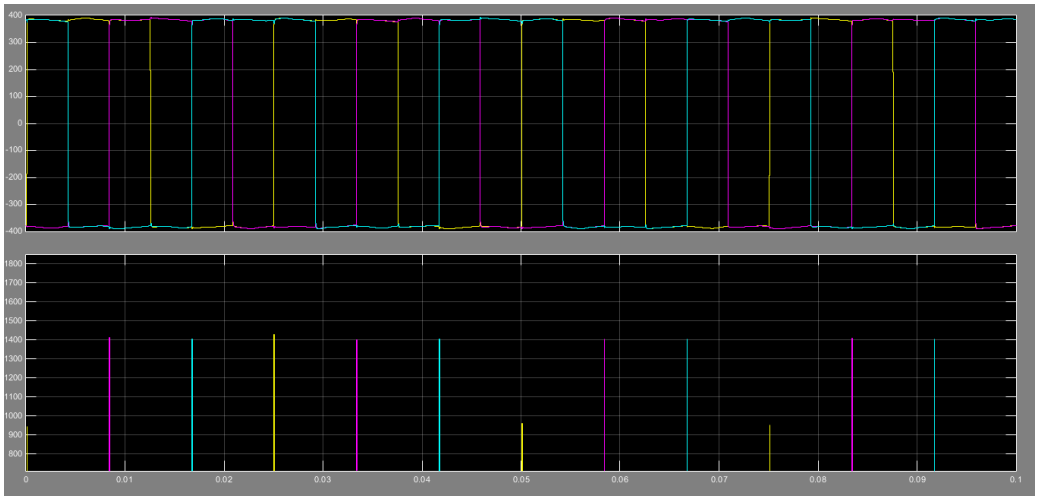

Fig. 6 Output of 3-level FCCMLI

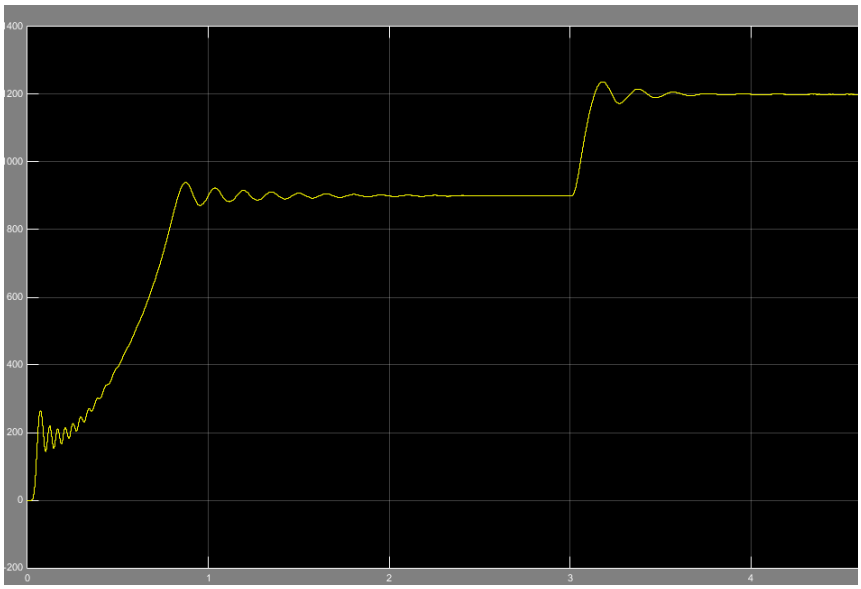

Fig. 7 Speed response of three phase induction motor

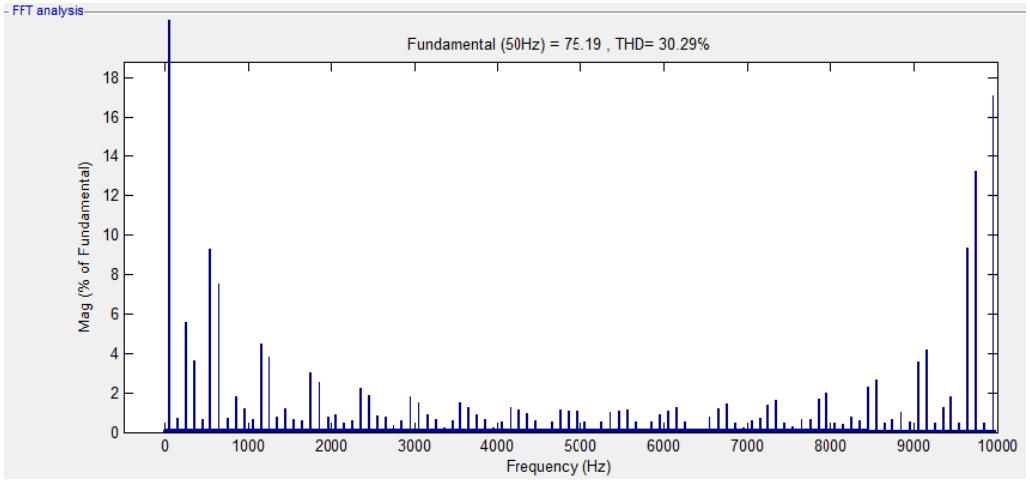

Fig. 8 Total harmonics distortion

VI. CONCLUSION

Three phase induction motor drive is simulated using MATLAB Simulink by using feedback system with SPWM modulation technique. From output result it is observed that speed of induction motor is maintained constant with the help of feedback system. With multilevel inverter harmonics in voltage waveform reduces. Ripples in current are also reduce when multilevel inverter is used. Losses are reduced. Keeping the cell- capacitor voltage differences within restricted voltage bands and so the capacitor voltages are balanced. The flying-capacitor inverter can operate with inherent capacitor voltage balancing. This drive system can be used in industries where adjustable speed drives are required to produce output with reduced harmonic.

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