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Design and Implementation of 4-Port Router

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Abstract- The Four Router Design is finished by utilizing of the three obstructs .the squares are 8-Bit Register, Router controller and yield piece. the switch controller is configuration by utilizing FSM plan and the yield square comprises of three fifo's consolidated together the fifo's are store parcel of information and when u need to information that time the information perused from the FIFO's. In this switch configuration has three yields that is 8-Bit size and one 8_bit information port it utilizing to drive the information into switch we are utilizing the worldwide clock and reset signals, and the fail flag and suspended information signals are yield's of the switch. The FSM controller gives the error and suspended_data_in signals.
Keywords-Network-on-Chip, FIFO, FSM, Register blocks, Simulation Router.

I. INTRODUCTION

This proposed inquire about paper is a Multiprocessor framework on chip is rising as another pattern for System on chip plan yet the wire and power outline limitations are driving appropriation of new outline philosophies. Scientists sought after a versatile answer for this issue i.e. Arrange on Chip (NOC). Organize on chip design better backings the incorporation of SOC comprises of on chip parcel exchanged system. Along these lines the thought is acquired from extensive scale multiprocessors and wide region arrange space and imagines on chip switches based system. Centers get to the system by methods for appropriate interfaces and have their bundles sent to goal through multichip steering way.

So as to execute a focused NOC engineering, the switch ought to be productively plan as it is the focal segment of NOC design. Plan and Verify the usefulness of the "Outline and Verification Four Port Router for Network on Chip" IP center utilizing the most recent check philosophies, Hardware Verification Languages and EDA devices and qualify the IP for Synthesis a usage.

The Four Router Design is finished by utilizing of the three blocks. They are 8-Bit Register, Router controller and fifo. The switch controller is configuration by utilizing FSM outline and the yield square comprises of three fifo's consolidated together the fifo's are store bundle of information and when u need to information that time the information perused from the FIFO's. In this switch configuration has three yields that is 8-Bit size and one 8_bit information port it utilizing to drive the information into switch we are utilizing the worldwide clock and reset signals, and the fail flag and suspended information signs are yield's of the switch The FSM controller gives the err and suspended_data_in signals.

II. LITERATURE SURVEY

90% of ASIC re-twists are because of Functional bugs. As the useful confirmation chooses the nature of the silicon, we burn through 60% of the plan process duration just for the check/recreation. With a specific end goal to dodge the postponement and meet the TTM, we utilize the most recent check techniques and advances and quicken the confirmation procedure. This venture helps one to comprehend the total useful confirmation procedure of complex ASICs and SOC's and it offers chance to attempt the most recent check

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techniques, programming ideas like Object Oriented Programming of Hardware Verification Languages and modern EDA instruments, for the fantastic confirmation.[1]

The store and forward stream instrument is best since it doesn't save channels and in this way does not prompt sit out of gear physical channels. The authority is of turning need conspire so that each channel once motivate opportunity to exchange its information. In this switch both information and yield buffering is utilized with the goal that blockage can be kept away from at both sides.

Highlights:

• Full duplex synchronous serial information exchange
• Variable length of exchange word up to 64 bytes.
• HEADER is the principal information exchange.
• Rx and Tx on both rising or falling
• edge of serial clock autonomously
• 4 beneficiaries select lines
• Fully static synchronous plan with
• One clock area
• Technology free VERILOG
• Fully synthesizable. [2]

III. METHODOLOGY

Block diagram of Router

Router Design Principles:

Router is a packet based protocol. Switch drives the approaching parcel which originates from the input port to output ports in view of the address contained in the packet. The router has a one information port from which the bundle enters. It has three yield ports where the data is driven out. The router has a dynamic low synchronous information reset which resets the switch.

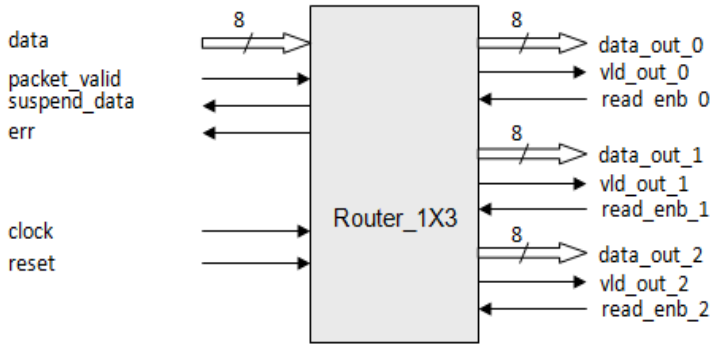

Figure 1 : Block Diagram of Four Port Router

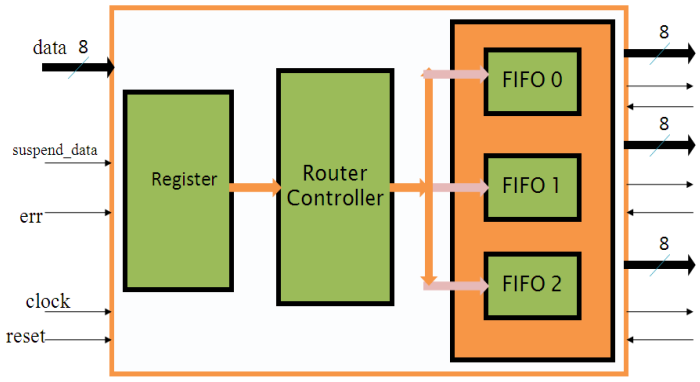

Figure 2 : Router Internal Structure

Information bundle moves into the info channel of one port of router by which it is sent to the yield channel of other port. Each info channel and yield channel has its own particular disentangling rationale which expands the execution of the switch. Cushions are available at all ports to store the information temporarily. The buffering technique utilized here is store and forward. Control rationale is present to settle on assertion choices. Subsequently correspondence is built up amongst information and yield ports.. As per the goal way of information bundle, control bit lines of FSM are set. The development of information from source to goal is

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called exchanging instrument The bundle exchanging system is utilized here, in which the bounce size is 8 bits .Thus the parcel measure changes from 0 bits to 8 bits.

Packet Format

Packet contains 7 parts. They are Header, payload and parity.

Packet width is 8 bits and the length of the packet can be between 1 bytes to 67 bytes.

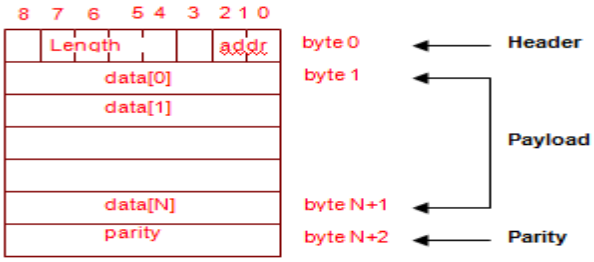

Figure 3 **:** Packet format

IV. IMPLEMENTATION

The four port router design is implemented by FSM controller. The FSM flow is shown below. In this FSM flow it has to direct the data to a particular FSM. Starting from the dec_add the data will go to the register block i.e, load_data0, load_data1 & load_data2.

FSM will check whether the fifo is empty or not. If it is empty then the data is load to fifo otherwise wait till fifo becomes empty. Finally the parity is checked at the output of the router. If the output receives same parity as that in the input then we can say correct data packet is transmitted.

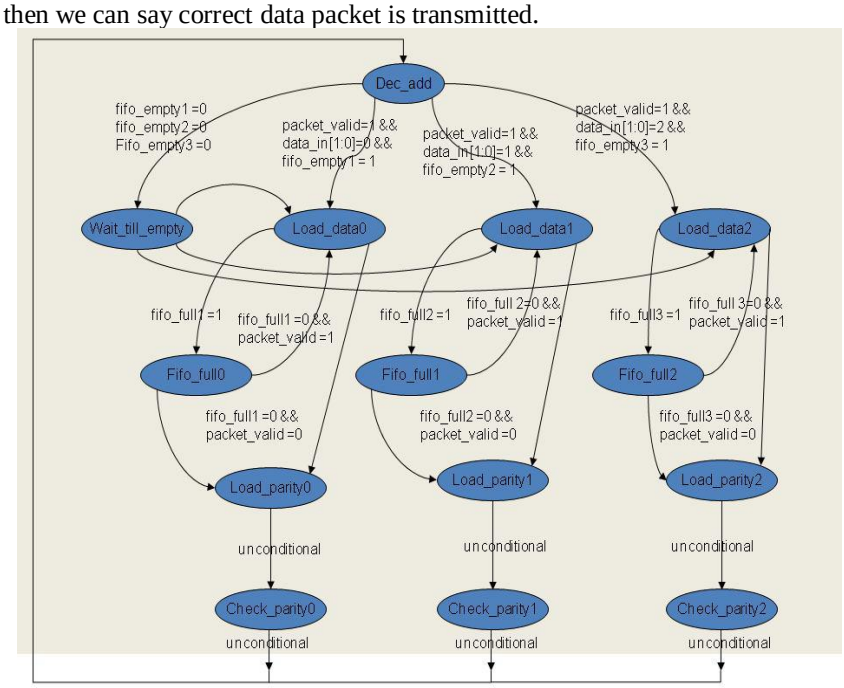

Figure 4 : FSM Overflow

V. EXPERIMENTAL RESULTS

The below figures shows the simulation results of test cases applied to the UUT. This is the simulation output of top router. In this we can merge all the 3 blocks such as fifo, FSM, register. As the packet valid is high the data is write in the input of router say 39, 24, 81, 09, 63 so on… and at the output the same 8-bit is received along with the parity. From the FSM controller that set the port too as high. So we can observe the data from fifo-2 of router.

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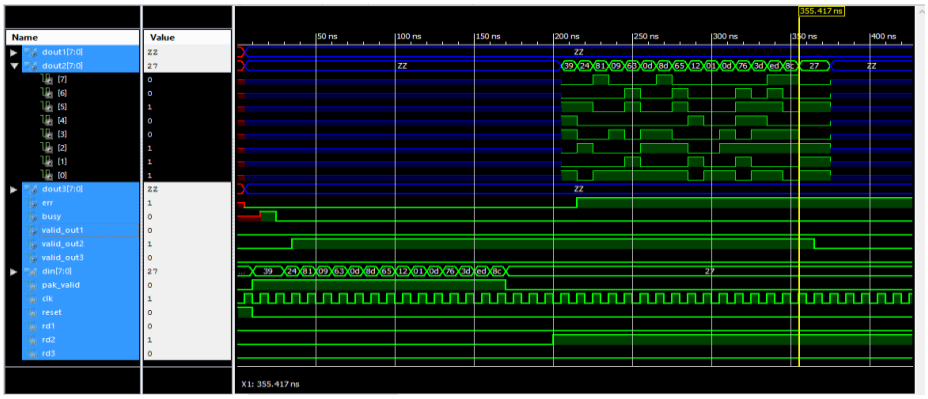

Figure 5: Simulation of top_router

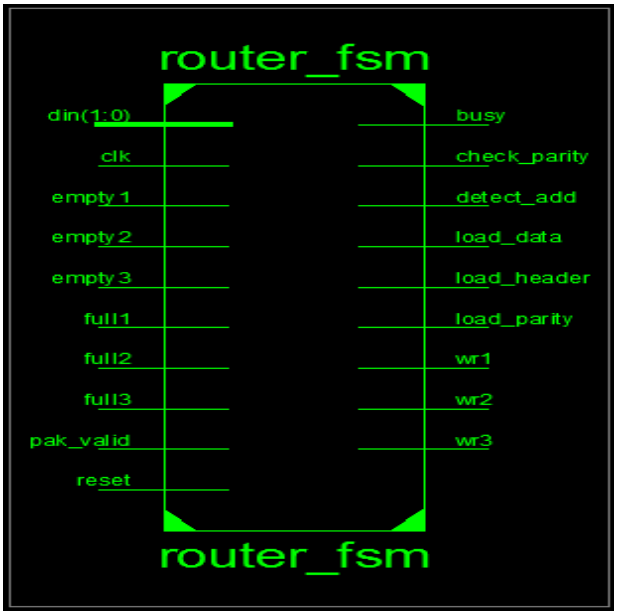

Figure 6: Synthesis of FSM block

In this Four Port Router project Design and verified the functionality of Router with the latest Verification methodology i.e. System Verilog. . In this I utilized one master and eight slaves to screen the Router.

VI. CONCLUSION

In this Four Port Router extend we Design and checked the usefulness of Router with the most recent Verification philosophy i.e., System Verilog and watched the code scope and practical scope of Router by utilizing cover points ,cross and diverse experiments like obliged, weighted and coordinated test cases. By utilizing these test cases we enhanced the utilitarian scope of Router. In this we utilized one master and eight slaves to screen the Router. Thus the utilitarian scope of Router was moved forward.

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