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# Design and Implementation of Memory Block using SRAM

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**Abstract- CMOS technology feature size and threshold voltage have been scaling down for decades for achieving high integration density and high performance. The continuing decrease in the aspect ratio and the corresponding increases in chip density and operating frequency have made power consumption a major concern in VLSI design. This paper provides the outline structures of Static Random Access Memory (SRAM) for low power dissipation with 6T AND 8T SRAM. The reason for attaining low power in the SRAM is by reducing the voltage at output node. The memory block of 4 BIT using 8T designed by 90nm technology with supply voltage of 1.2V. It is implemented by using synopsys tool using custom compiler.**

**Keywords- CMOS, SRAM, SENSE AMPLIFIRE,DECODER.**

## I. INTRODUCTION

In current years, a high-speed blooming in the field of VLSI has led to reduced device structures & increased transistors bulk of integrated circuits & circuits with high complications. Such designs utilize an extra amount of power and produce an increased amount of heat. Due to these matters, circuit planners are realizing the significance of limiting power consumption & improving energy efficiency at all levels of the designs.

### 1.1 About front end design tool

Silicon chip are the best foundation for everything like mobile phones to smart wearable medical devices to self-driving vehicles (autonomous cars), hence the complexity of system increases therefore the SYNOPSYS is best solution for designing the complex chip .To achieve the best quality and productivity of devices **Synopsys**

 

**design platform** is very essential because it provides the design of advanced digital ,custom & analog\mixed signal very quickly with best power ,performance, area (PPA).

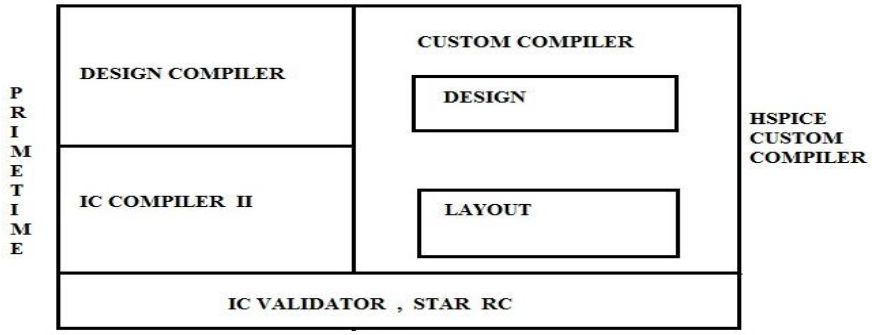


Fig 1: Synopsys Design Platform.

Design compiler:

It reads the RTL design (verilog, SV, VHDL) to generating a final gate level net list

IC compiler:

Which provides the complete place and route system that enables the 10X faster throughput design to address today's high time to market pressure during the best –in-class solution for flat & hierarchical design planning

IC validator:

Which provides the physical verification solution, high performance DRC &LVS substantially reduced time to results.

Star RC:

This is used as solution to achieve the high performance parasitic extraction for IC implementation and design. Also provides the industry-leading performance &capacity for user's extraction of gate –level and transistor level, supports simultaneous multicorner extraction (SMC) Which allows to increasing No. of extraction corner with single run time with less disk usage and runtime.

Custom Compiler:

It is the full custom design solution, which has the visually –assisted automation features flow to speed up common design task, reduced iteration & enable reuse. It eliminates the need to write complicated codes and constraints with custom compiler, routine & repetitive task are dealt with automatically without extra setup

## II. METHODOLOGY

**Conventiona6T SRAM :**

The schematic of the conventional 6T SRAM full is shown in Fig 2.

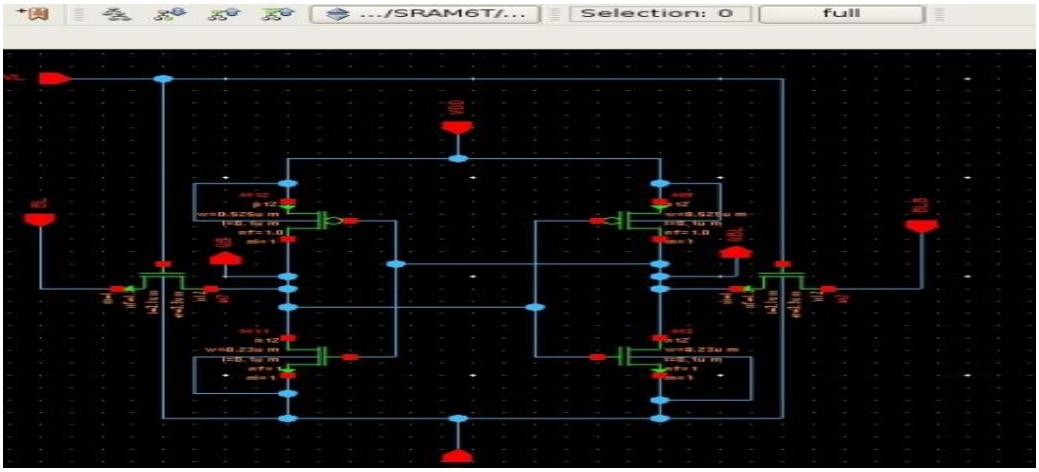


Fig 2: Conventional 6T SRAM

 

The traditional SRAM 6T cell consists of two cross coupled CMOS inverters with two access transistors attached to supportive bit lines. Fig1 shows below the circuit diagram of a SRAM 6T cell [3]. Fallowing operation are perform by SRAM.

Read Operation
Pre charge Bit-lines (BL), BLB (Bit-line bar) to VDD. Turn on WL (Word line). BL or BLB will pull down to low depending on storage node QD and QB
Write Operation
Drive bit line (BL), bit line bar (BLB) with necessary values (0,1 or 1,0). Turn on word line, bit lines (BL or BLB) over power cell with new value.

## PROPOSED 8T SRAM:

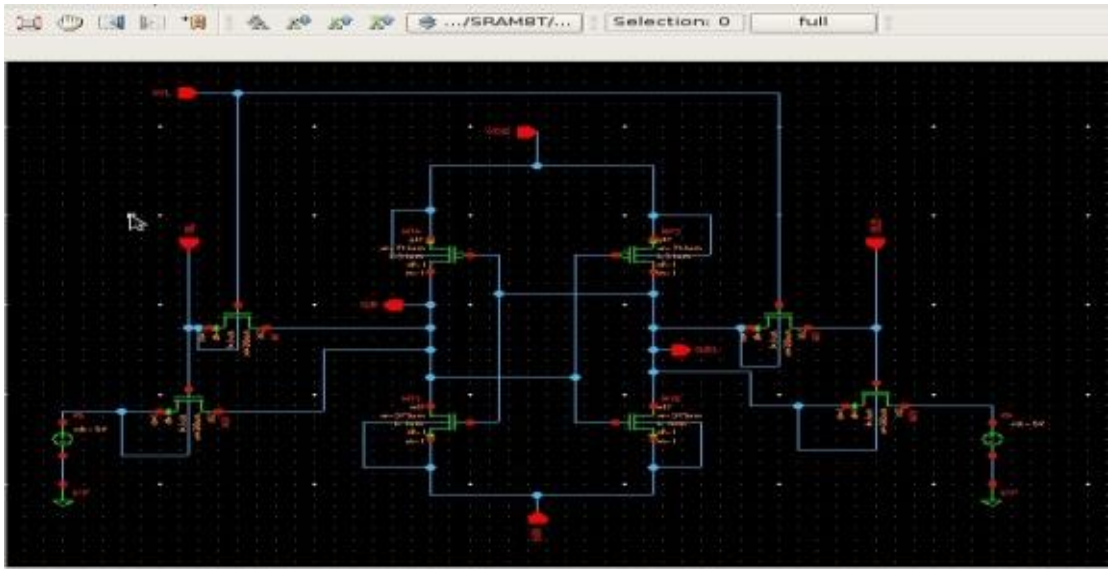


**Fig 3: schematic of 8T SRAM**

Schematic of 8T SRAM shown in Fig 3. It work similar to 6T SRAM BUT It is reduce the signal swings on the capacitive nodes like bit lines and bit bar lines

## MEMORY UNIT 8T SRAM

**To design memory requires fallowing circuits**

**1. Write driver**
**2. precharge**
**3. Sense amplifier**
**4. decoder**

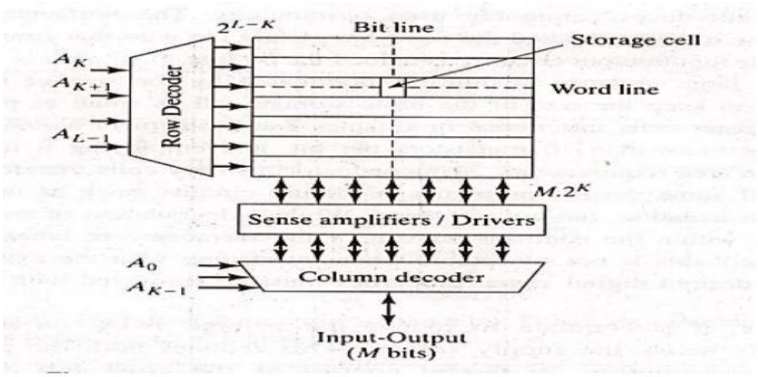


**Fig 4: basic memory block**

 

Decoder are used for enabling each memory cell which stores single bit of data. Precharge is use to keep bit line and bit bar line to vdd after every operation.

## III. DESIGN & IMPLEMENTATION OF 8T SRAM of 4 BITS MEMORY CIRCUIT

To implement 4 bit SRAM memory a 2-4 row decoder and 2-4 column decoders is used. It is arranged in 4x4 matrixes (SRAM 8T cell) form. Here the outputs of the row decoder are connected to the SRAM cells word line 'wl' and the bit lines of all cells are connected to the column decoder. When the input to the decoder is 00, the word line 'wl' of first row become high and all the SRAM cell are connected to the bit line. But depending upon the address of the column decoder one column will be chosen. In this way a particular cell of the SRAM memory array will be picked. For example if '00'will be the address for both row decoder and column decoder, then a particular cell whose location is '00' in the memory array will be selected. If address of the row decoder is '00' but the address of the column decoder is '01' then second SRAM cell of the first row is selected. Fig 6 shows the schematic of 4 bit sram cell. Simulations have been performed using SPICE based on SAE( Simulation and Analysis Environment) 0.9µm CMOS technology with supply voltage of 1.2V.

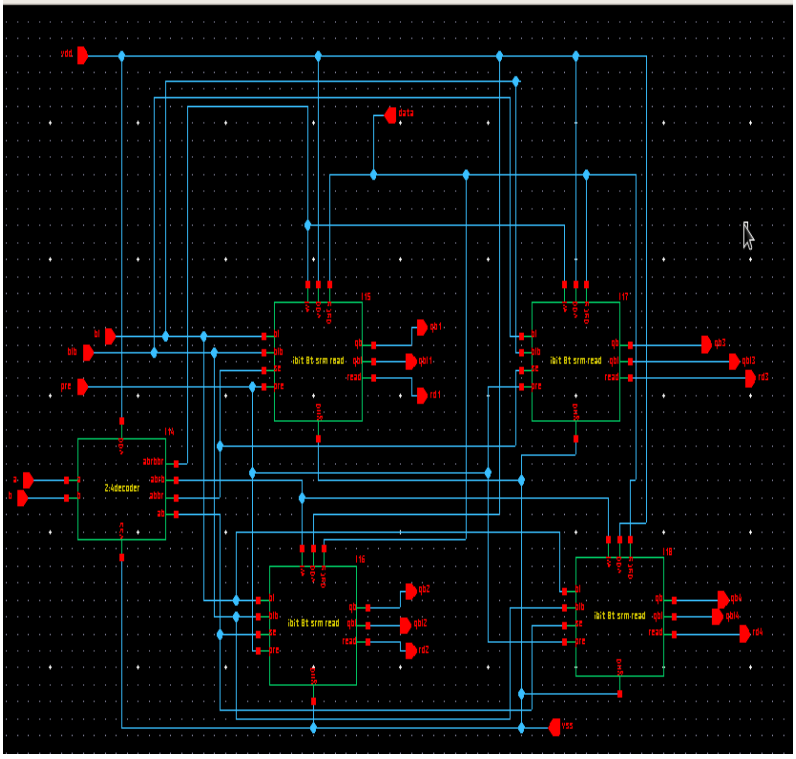

Fig 5: Proposed 8T 4 bit SARM memory unit

## IV. EXPERIMENTAL RESULT

Output wave forms of conventional and proposed 6T SRAM are shown in Fig 6 and Fig 7.

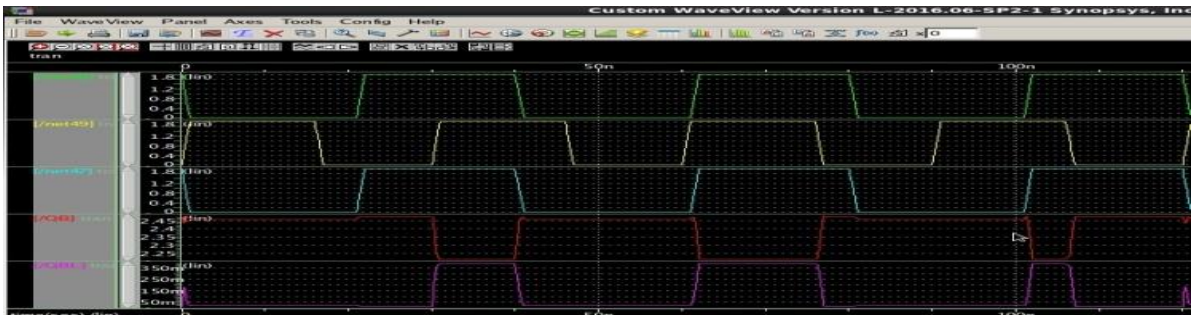

Fig 6: Output Waveform of Conventional 6T SRAM

 

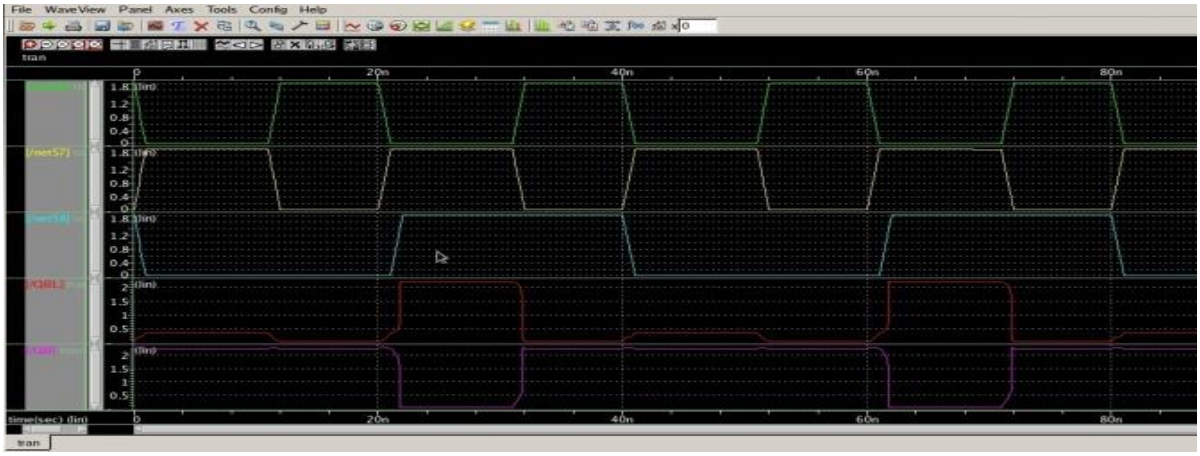

Fig 7: Output Waveform Of Proposed 8T SRAM.

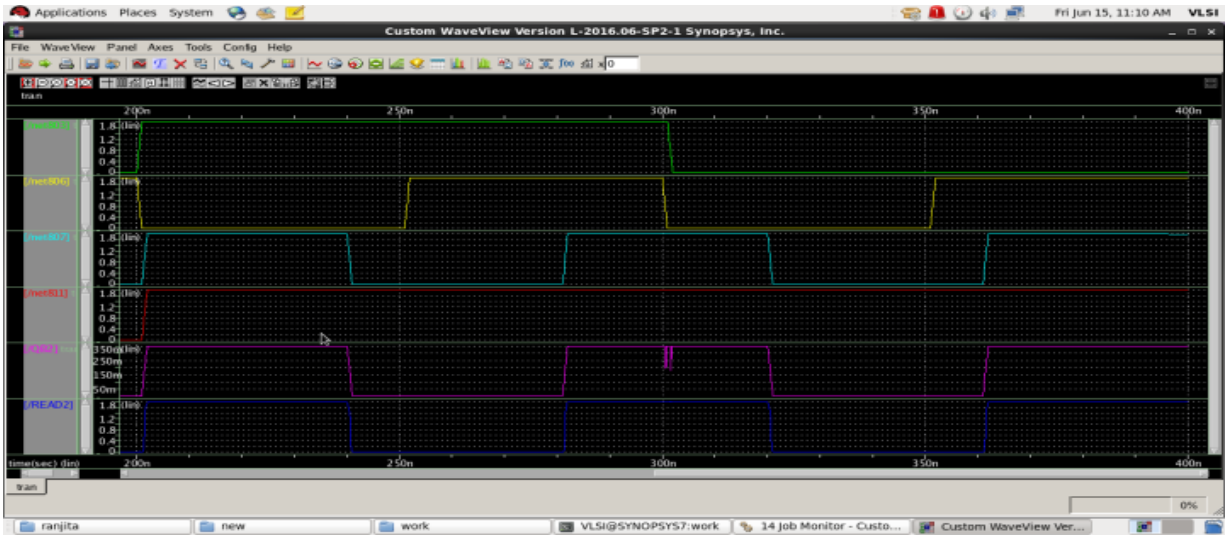

Fig 8: Output Waveform Of 4BIT MEMORY

**Tabulation of Simulation results:**

**Table 1: POWER DISSIPATION**

| Supply Voltage (V) | Power Dissipation(W) |
|---|---|
| 1.2 | 0.845pW[6T SRAM]<br>0.694Pw[8T SRAM] |

## V. CONCLUSION

Proposed work consists of SRAM memory design using SYNOPSYS TOOL, observed that SRAM 8T cell dissipates less power in comparison to 6T transistor SRAM cell as the temperature rises. The SRAM 8T transistor SRAM cell dissipates less power at different power supply voltages in comparison to SRAM 6T cells. As the supply voltage down the power dissipation also reduced. The 8T transistor SRAM dissipates less power at higher bit-line capacitance in comparison to SRAM 6T transistor. Implemented the 4bit memory unit.

 

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