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RESEARCH ARTICLE

A NOVEL DESIGN OF REVERSIBLE FLOATING POINT ADDER ARCHITECTURE

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Abstract — This project revolves around the design and implementation of floating point adder architecture using reversible logic to improve the design in terms of the number of garbage outputs and the number of gates used. In recent years, reversible logic has emerged as a promising technology having its applications in low power CMOS, quantum computing, nanotechnology and optical computing because of its zero power dissipation under ideal conditions. In this paper, the reversible logic closely follows the IEEE754 specification for binary Floating point adder architecture is done so as to minimize the number of gates used and their garbage outputs. The existing and the proposed floating point adder architectures are designed using Verilog and simulated using Xilinx ISE 9.1 tool.

Keywords— Reversible Gate, Garbage Outputs, Constant inputs, Quantum Cost

1. INTRODUCTION

In modern VLSI systems, power dissipation is very high due to rapid switching of internal signals. It has been shown that for every bit of information lost in irreversible logic computations, kT*log2 joules of heat energy

is generated, where k is Boltzmann's constant and T is the absolute temperature at which computation is performed. But this power dissipation can be avoided if the circuit is made reversible by using reversible gates in place of conventional logic gates. A reversible circuit is one in which the inputs can be reproduced from the outputs and vice versa. A gate is considered to be reversible only if for each distinct input there is a distinct output assignment. The inputs to reversible gates can be uniquely determined from its outputs. A reversible logic gate must have the same number of inputs and outputs. A reversible gate is balanced, i.e. the outputs are 1s for exactly half of the inputs. A circuit without constants on its inputs and composed of reversible gates realizes only balanced functions. It can realize non balanced functions only with garbage outputs. Garbage outputs are those outputs that are not used as inputs to other circuit blocks. Some of the major problems with reversible logic synthesis are that fan outs cannot be used, and also feedback from gate outputs to inputs is not permitted [3]. Reversible gates have applications in Nuclear Magnetic Resonance (NMR), quantum computation, Quantum dot Cellular Automata (QCA), and optical computing. The most prominent application of reversible logic lies in quantum computers. A quantum computer will be viewed as a quantum network (or a family of quantum networks) composed of quantum logic gates. The main objective of this project is to design and implement a floating point adder architecture such that,

- Minimum number of gates are used for implementation
- The number of garbage outputs are restricted to as few as possible
- Minimum number of constant inputs are used

Following are the need of reversible circuits:

- To reduce the amount of heat dissipation due to information loss in irreversible circuits, reversible circuits are used.
- Reversible logic circuits are in demand for high speed power efficient circuits and are needed to recover the state of inputs from outputs.
- Reversible computing will lead to improvement in energy efficiency which will eventually affect the speed of most computing applications.
- To increase the portability of devices again reversible computing is required [4].

2. DIFFERENT TYPES OF REVERSIBLE LOGIC GATES

2.1 Not Gate

The simplest reversible gate is the NOT gate and it is a 1*1 gate. This NOT Gate has a Quantum Cost of zero and is as shown in Fig 1.

Fig.1: NOT Gate

2.2 Peres Gate

The Peres gate is a 3*3 reversible gate having inputs (A, B, C) mapped to outputs (P = A, Q =A^B, R = (A*B)^C).This gate has a Quantum cost of 4 and is as shown in Fig 5.

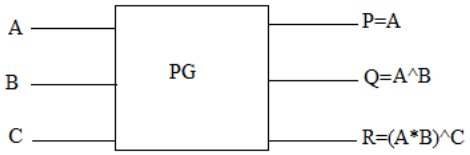

Fig.2: Peres Gate

2.3 Fredkin Gate

The Fredkin gate is a reversible 3*3 gate that maps the inputs (A, B, C) to the outputs (P=A, Q=A'B^AC, R=A'C^AB).This gate has a Quantum cost of 5 and is as shown in Fig 6.

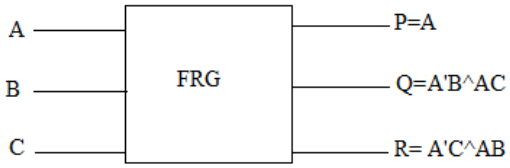

Fig.3:Fredkin Gate

2.4 HNG Gate

The HNG gate is a reversible 4*4 gate that has mapping inputs (A,B,C,D) to the outputs is (P=A, Q=B, R=A^B^C, S=(A^B)&C^AB^D). This gate has a quantum cost of 13 and is as shown in Fig 6.

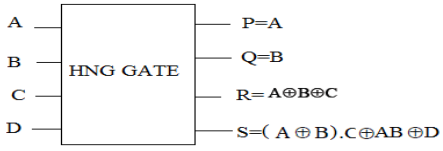

Fig.4: HNG Gate

3. EXISTING METHOD

In the existing method, a Floating point adder architecture was implemented using Feynman ,Toffoli, HNG , Peres and Fredkin gates. The designed Floating point adder architecture Block diagram is shown in figure 3.3, In this circuit, Reversible full adder circuits are used to construct a reversible Floating point adder architecture. In this architecture used IEEE754 specification. Using floating-point numbers garbles the results of these operations, due to a round-off error propagation. At the end of the computation, the result can be totally different of the expected result. In this architecture contains the reversible full subtractor circuit also to designed a Conditional Swap unit. Each of the full subtractor circuit produces the garbage outputs and therefore the total garbage output generated from the conditional swap is 19**.**

Here, the full subtractor is realized using (HNG) and Fredkin Gates. where the Conditional swap has a Quantum Cost is 238. In this implementation, a reversible full subtractor is implemented using two gates. So each full subtractor consists of four gates and its Quantum Cost amounts to 238. Fig 8 shows the full subtractor circuit.

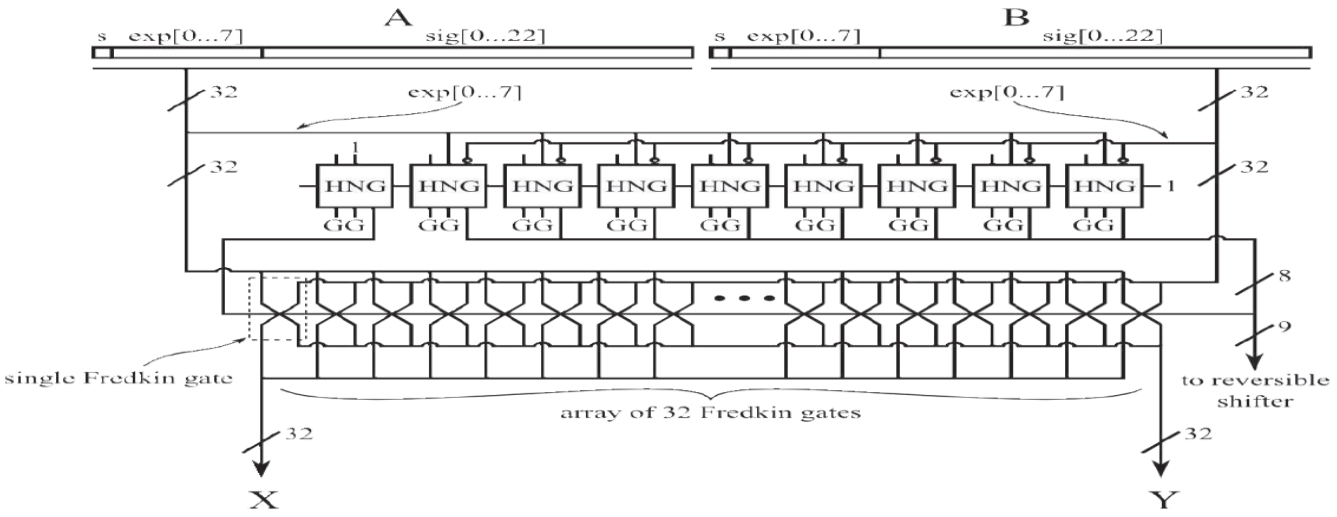

Fig.7:Conditional swap unit, A Combination Of HNG And Fredkin Gates

After the sign-magnitude to two's complement conversion, the addition is done by a reversible adder which is constructed from 27 RFA (Reversible Full Adder) gates and one RHA (Reversible Half Adder) gate in Fig :8

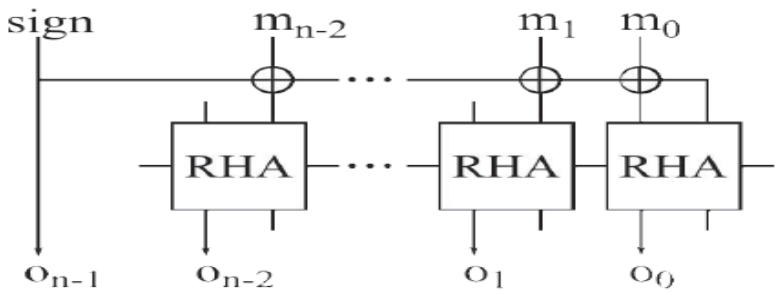

Fig. 8: Reversible Half Adder

The Reversible design requires regular repetition and interconnection of a primitive reversible cell design. The quantum implementation and block diagram of our proposed reversible leading zero counter (RLZC) it shows the fig:3.9 using an eight bit example–how multiple copies of the RLZC are interconnected to create the full reversible leading zero counter unit (RLZCU) that asynchronously produces the shift amount. For an *n* bit input operand, an ($n=2k$, k) reversible leading zero counter unit (RLZCU) requires $n-1$ RLZCs and $n-k-1$ Feynman gates for wire fan-out. After the addition, the result may have a number of leading zero bits or have one more bit with value of one at the most significant bit (MSB). The normalization is needed to adjust the result so that it conforms to the floating-point number format. In normalization, if a shift is required, it is either a one place right shift or a multiple place left shift. If the MSB has a value of one, one place of right shift takes place and the 8-bit exponent is passed through a reversible conditional increment unit. Otherwise, one or several places of left shift is needed in conjunction with a corresponding decrement of the 8-bit exponent

4. PROPOSED METHOD

The proposed method revolves around the design of a Floating point adder architecture using reversible logic gates such as Fredkin gate (FRG) , Feynman (FG) gates and Peres gate (PG).In this architecture included the Barrel shifter. A barrel shifter receives an *n*-bit input data value along with *k*-bit shift value and will produce an *n*-bit shifted result, The shift value can be either positive or negative and can be coded into 2's or 1's complement coding. Positive and negative shift values indicate unidirectional and bidirectional shifter/rotator respectively.

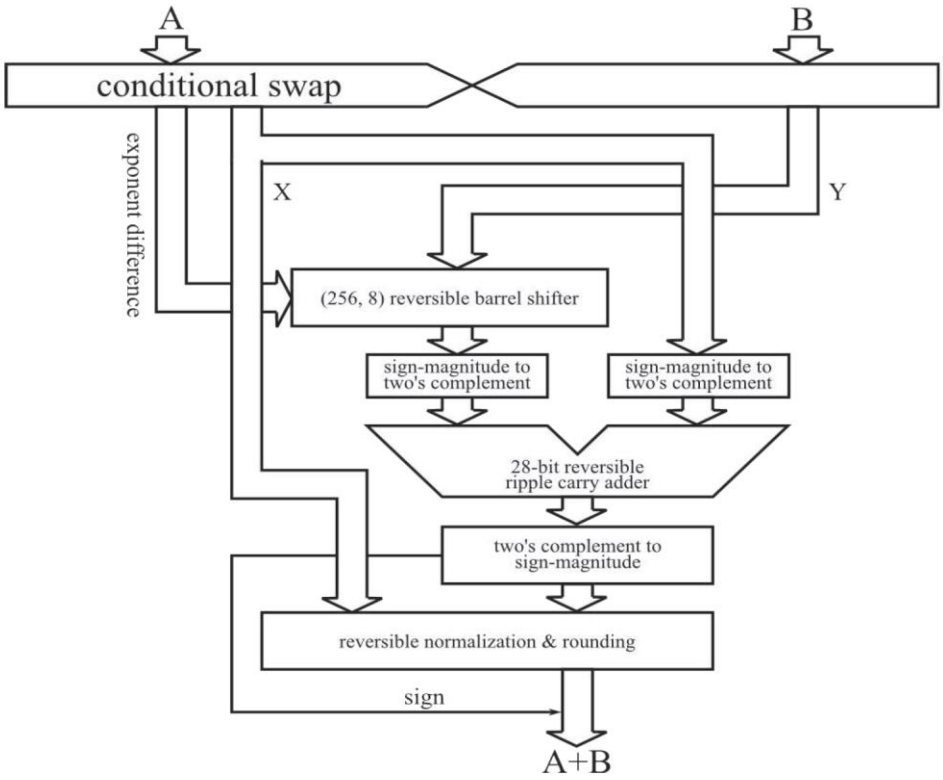

Fig.11:Floating point Adder Architecture

5. RESULTS AND OBSERVATIONS

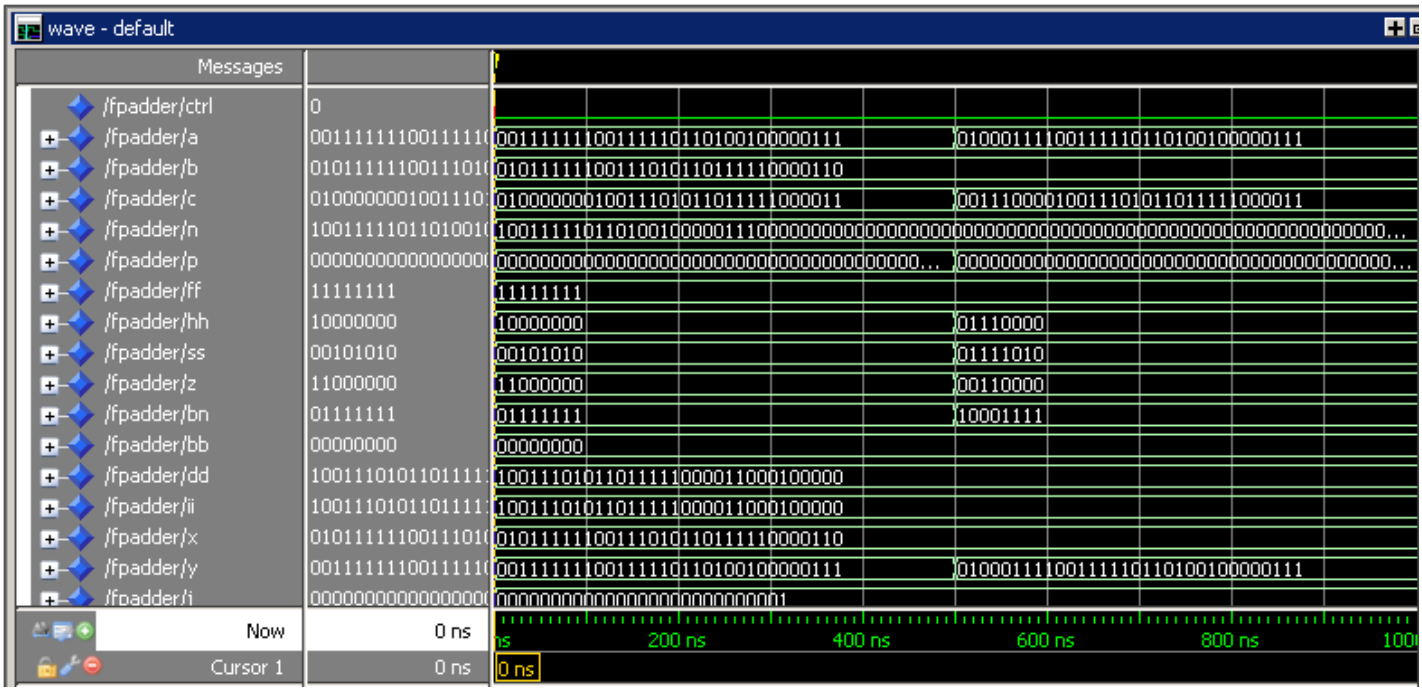

Fig.12: Waveform For Proposed Method

The following table shows Floating point adder architecture and proposed method in terms of the number of quantum costs and their garbage outputs.

TABLE.1: Proposed Reversible Floating point adder architecture Decomposed method

Floating point Adder	Number of Quantum costs	Number of Garbage outputs
Conditional Swap	234	18
Alignment	425	2260
Addition	165	55
Conversion	413	85
Normalization	2008	498
Rounding	0	9

From the above table, it can be seen that in the Proposed Floating Point Adder Architecture is used which is the exact half of that used in the Existing method.

6. CONCLUSION AND FUTURE WORK

Thus the Proposed method was designed and was found to be more efficient than the Existing method in terms of the number of gates used in the circuit. The Proposed method can be used to realize more complex circuits.

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