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RESEARCH ARTICLE

Design of Power Optimization using C2H Hardware Accelerator and NIOS II Processor

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Abstract— The current trend in the silicon industry has been a move steadily towards Chip Multicore Processor (CMP) system to get better outputs. However, chip multicore processors have higher amount of soft errors, which result in degradation of the overall system reliability. Hence, we have been cautious of using CMP architectures for faster-reliable embedded real-time system applications that have high reliability levels. The major use of these processors also states the processor migration tendency. With new technology processor architectures, the older ones are to become vanished sooner. Present the power optimization and detailed reliability analysis of power optimization of single-core and multi-core based systems. The analysis results are then used to compare the power optimization and reliability of CMP architectures with the corresponding reliability of single processor architectures.

To fulfil this requirement, Designs a method for power optimization using NIOS II processor. Reducing power consumption in embedded system that use Field programmable gate array (FPGA) is increasingly important, particularly for battery powered applications or to reduce heat or system cost. You can use parallel algorithms to exploit the parallel architecture of FPGA devices to accomplish more work per clock cycle, allow you to lower the clock frequency per frame. High-level development tools such as System On Chip Peripherals (SOPC) Builder and the NIOS II C-to-Hardware Acceleration Compiler (C2H) has tremendously useful in the power-saving potential of the FPGA hardware by easily adding hardware accelerators and lowering clock frequencies, optimizing power.

Keywords— Chip Multicore Processor; NIOS II Processor; C2H Compiler; FPGA; SOPC

I. INTRODUCTION

Recent years have seen the growth in embedded computer systems. Nowadays these systems have become ubiquitous. A significant number of embedded applications must meet power budgets. This has led to research in high level power estimation techniques and low power design for these specific systems. One challenge posed by the increasing transistor density on these chips is that the probability of soft errors and hard errors increases. In fact, research suggests that along with the growing likelihood of soft errors on CMPs, the probability of hard faults is also increasing. Hence, the safety critical industry has been wary about making the move to the CMP architecture in spite of the increasing computational requirements of current safety critical systems. The problem

is that the safety-critical industry is reaching the point where it will have completely exploited the computing power of single processor architectures for the growing software responsibilities and, hence, the industry is investigating architectures that will alleviate some of the concerns posed by CMP chips in meeting the standards of various certification authorities. When large FPGAs were launched into the market and stable software for developing embedded processing systems was released for these devices, the era of the embedded systems on FPGAs started and the system-on-a-chip for FPGAs. There are hard and soft processor cores for FPGAs. Soft cores can come in an HDL or they can be net lists generated from a specific EDA tool like Altera SOPC Builder and Xilinx EDK. The CMP processors can certainly enter the safety critical industry for some less critical functions for aircrafts, automobiles, or spacecraft's, to build a track record.

This paper presents a power and energy evaluation for different data and instruction caches sizes on a NIOS II FPGA Based embedded soft-core processor. Besides power, performance is also considered, as well as execution time and area. The results are based only on laboratory measurements. Although the study was done on a Cyclone III FPGA, the idea is to extract general conclusions for embedded processors on programmable logic.

II. EVALUATION SET UP

This paper evaluates the power and energy consumption of the NIOS-II embedded processor on a Cyclone III development kit from Altera. The software suite used for FPGA synthesis and implementation is the Quartus-II v11.1.The NIOS-II IDE v6.1 and the GCC compiler was used for editing and compiling the benchmark programs. The specific parts in the evaluation board used in this work are the Cyclone IV EP4CE115F29C7 and the Micron DDR SDRAM MT46V16M16P-6T.NIOS-II is a 32-bit RISC embedded processor that can be tailored to a broad range of applications. There are three different types of cores available for the user: small, standard and fast. The small and standard cores have a narrow set of configuration parameters and focuses on low demanding computing applications.

Power consumption is analysed with 5 Accelerator as shown in block diagram below.

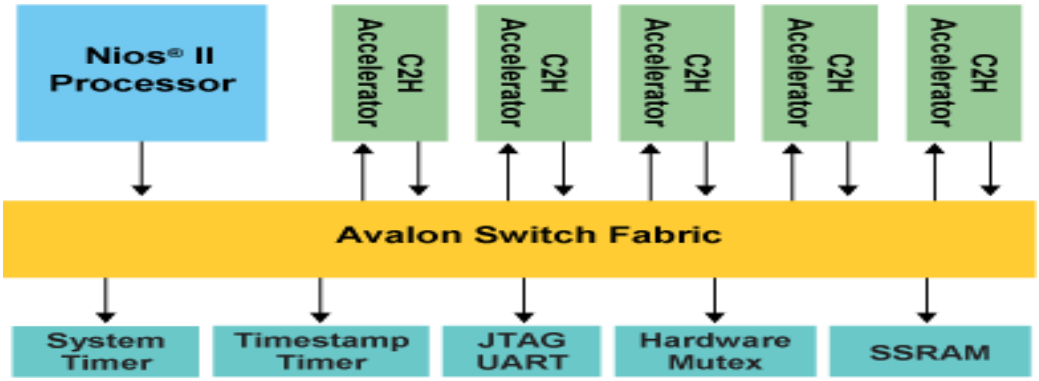

Figure 1. Block Diagram

Here we have design a Verilog program for power consumption by using 5 accelerators, Avalon switch fabric, NIOS II processor and SRAM. The results for power optimization are obtained from QUARTUS II Software. QUARTUS II Software consists of tool known as power play power analysis tool which is use for analysis of power.

III. NIOS II PROCESSOR

NIOS II is a 32 bit reserved instruction set soft core processor which is use for multi functionality and faster use which also helps to reduce power required for execution of function. Like the original NIOS, the NIOS II architecture is a RISC soft-core architecture which is implemented entirely in the programmable logic and memory blocks of Altera FPGAs. The soft-core nature of the NIOS II processor lets the system designer specify and generate a custom NIOS II core, tailored for his or her specific application requirements. System designers can extend the NIOS II basic functionality by adding a predefined memory management unit, or defining custom instructions and custom peripherals. Similar to native NIOS II instructions, user-defined instructions accept values from up to two 32-bit source registers and optionally write back a result to a 32-bit destination register. By using custom instructions, the system designers can fine-tune the system hardware to meet performance goals and also the designer can easily handle the instruction as a macro in C. NIOS II is offered in 3 different configurations: NIOS II/f (fast), NIOS II/s (standard), and NIOS II/e (economy).

IV. C2H HARDWARE ACCELERATORS

The NIOS II C-to-Hardware Acceleration (C2H) Compiler is a tool that allows you to create custom hardware accelerators directly from ANSI C source code. A hardware accelerator is a block of logic that implements a C function in hardware, which often improves the execution performance by an order of magnitude. Using the C2H Compiler, you can develop and debug an algorithm in C targeting an Altera NIOS II processor, and then quickly convert the C code to a hardware accelerator implemented in a field programmable gate array (FPGA). The C2H Compiler improves the performance of NIOS II programs by implementing specific C functions as hardware accelerators. The C2H Compiler is not designed to create arbitrary hardware systems from C code. Rather, the C2H Compiler is a tool for generating a hardware accelerator module, functionally identical to the original C function that offloads and enhances the performance of the NIOS II processor. The NIOS II C-to-Hardware Acceleration (C2H) Compiler represents Altera's next step in the evolution of embedded systems design. The C2H Compiler uses the infrastructure provided by SOPC Builder and the NIOS II processor, and adds a higher level of abstraction converting C functions directly to hardware.

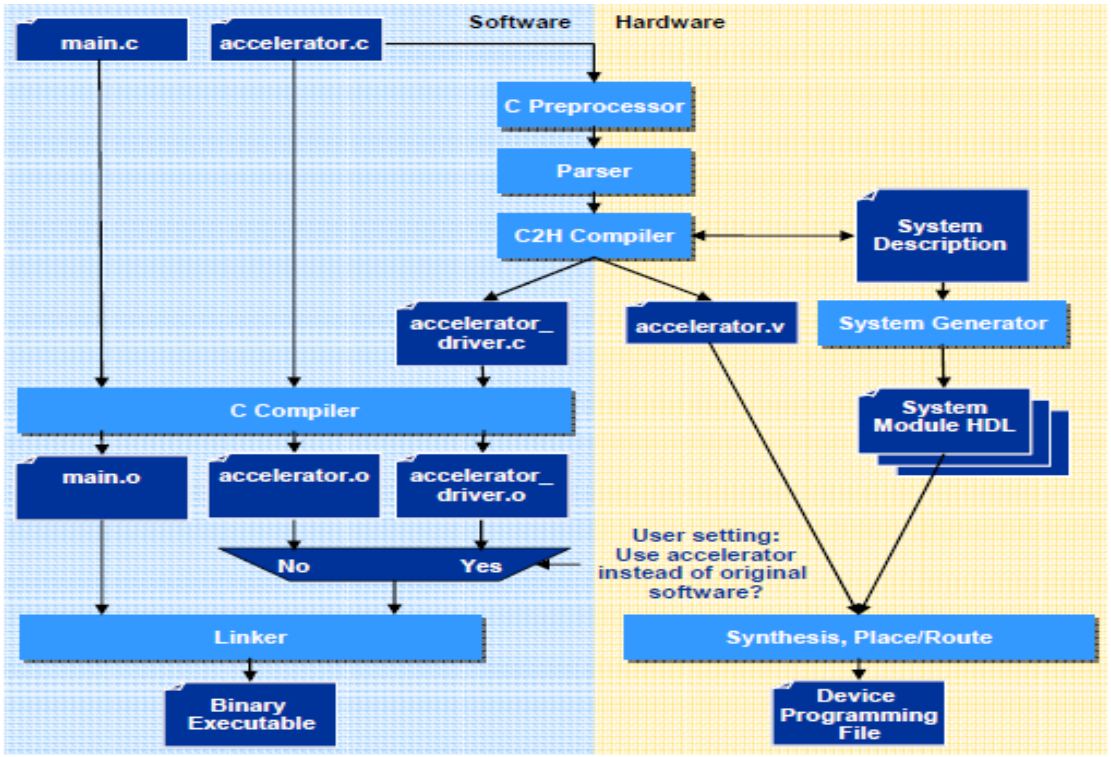

Figure 2. C2H Integration with Software Build

V. RELATED WORK

[1] This paper discusses the power consumption of NIOS II embedded processors on various FPGA (Field Programmable Gate Array) platforms. Power and energy consumption have been measured using an automated test bench. From these measurements, parameters with the greatest influence on the power and energy consumption are identified, and power and energy models are developed. Those models will be included in high level tools for early design space exploration. They exhibit a relatively low error (3% in average). They were validated against measurements on a video analysis application. The works which are presented here have been undertaken in the frame of the Open-PEOPLE research project, which goal is to provide a platform dedicated to power and energy measurement, estimation and optimization for complete embedded systems.

[2]This paper proposed Transient faults in chip multiprocessors are an emerging problem as power and performance demands push semiconductor technologies to their limits.

As transistors shrink with each new generation of many core processors, allowing for more cores on each chip, soft errors will increase considerably. To address this problem, A new and practical systems approach of managing and allocating reliability according to software process requirements. The asymmetric multi-

core architecture is based on cores with differing reliabilities. Critical and non-critical software components are identified and matched with the higher reliability cores. We show that by using asymmetrically reliable cores the overall system failure rate can be reduced by several times when critical processes can be isolated and executed by higher reliability cores, while offering the same or better overall performance, power utilization and chip area as symmetric cores.

[3]This paper is a study of the NIOS II power characterization. The relationship between instruction and data cache sizes and the corresponding energy consumption is analysed. The study is based on more than one thousand current measurements for different benchmark programs and cache configurations. From the results it is clear that using the optimal cache sizes leads to the lowest energy consumption even when considering execution time, power, and FPGA resources utilization. As an additional result the paper shows an example where the use of integer instead of floating point operations can save a significant amount of energy. Lastly, it is shown that the energy consumption as a function of the input data size follows the same function as the computational complexity for the studied examples.

[4].This paper reports the impact of different NIOS II hardware and software options for arithmetic operations on its power and energy consumption. These options are evaluated on the Cyclone II and Stratix II FPGA families using a number of benchmark programs. This analysis is part of a more complete study oriented to characterize the power and energy consumption of an embedded processor like the Altera's Nios II. Results are based on physical measurements and show significant energy savings and higher performance in arithmetic operations when available arithmetic hardware suitable for these operations is included. However when the utilization of resources is taken into account, then setups with less hardware and more software for arithmetic computation can be more efficient.

[5] This paper compares typical safety-critical architectures and investigates the reliabilities of different CMP architectures. We present the fault tolerance framework and detailed reliability analysis of fault-tolerant single-core and multi-core based systems. The analysis results are then used to compare the reliability of CMP architectures with the corresponding reliability of single processor architectures. Although a CMP system does encounter degradation, by applying some system level dependability assurance mitigation features, its reliability can be enhanced. This enables CMP systems to be effectively deployed in critical applications.

[6] This article discusses the application of the NIOS II processor in a PFC converter. This processor was provided by ALTERA to be implemented in FPGA. The FPGA is capable of a parallel processing and hardware modification, and also offers the possibility of microprocessor implementations, which can be programmed in Assembly or C. The NIOS II is a versatile embedded processor family that has a high performance and was created for FPGA. This processor family consists of three processor cores that implement a common instruction set architecture, each optimized for either a specific cost or performance, and all supported by the same software tools. The NIOS II Processor propitiates flexibility such as: selecting the exact set of CPUs, peripherals, and interfaces, accelerating only relevant functions and eliminating the risk of processor obsolescence. The focus of this paper is the use of this processor applied to the digital control of a single-phase pre-regulated rectifier, showing the advantages and disadvantages of the use of this technology. The control strategy used aims to obtain Power Factor Correction (PFC) of a single-phase voltage doublers rectifier with a centre tap at the voltage output. The FPGA used in this study is an ALTERA Cyclone II EP2C35F672C6.

VI. **DISCUSSION & FUTURE WORK**

On further investing we can develop enhancing the reconfigurable multicore processor to increase the speed of the system and to design multiple numbers of C2H hardware accelerator by designing their programing in C source code and developing accelerator using NIOS IDE software tool and then implementing them on FPGA kit. We are also going to calculate the Mandelbrot fractal algorithm calculations which use for proper calculation of power used in system. Further we are also going to compare the result on different numbers cyclone FPGA boards so that we can get the clear idea of the comparison of results and conclude that which one is better for power optimization results and check whether that further increase in the accelerator what performance do we get.

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